

Complex Detector Electronics: FPGA's & ASIC's

Complex systems and experiments with very high channel counts need to make a large number of logical decisions rapidly. Options for “electronic decision makers” include: a microprocessor (in CAMAC or VME), a field-programmable gate-array (FPGA), or an application-specific integrated-circuit (ASIC).

<http://www.tutorial-reports.com/computer-science>

	performance	NREs	Unit cost	TTM
High ↑	ASIC	ASIC	FPGA	ASIC
Low	FPGA	FPGA	MICRO	FPGA
	MICRO	MICRO	ASIC	MICRO

ASIC = custom IC, MICRO = microprocessor

NRE's – non-recurring engineering costs

TTM – time to market

FPGA's ... the manufacturer

<http://www.xilinx.com/>

ASIC's ... the website:

<http://www-ee.eng.hawaii.edu/~msmith/ASICs/HTML/ASICs.htm>

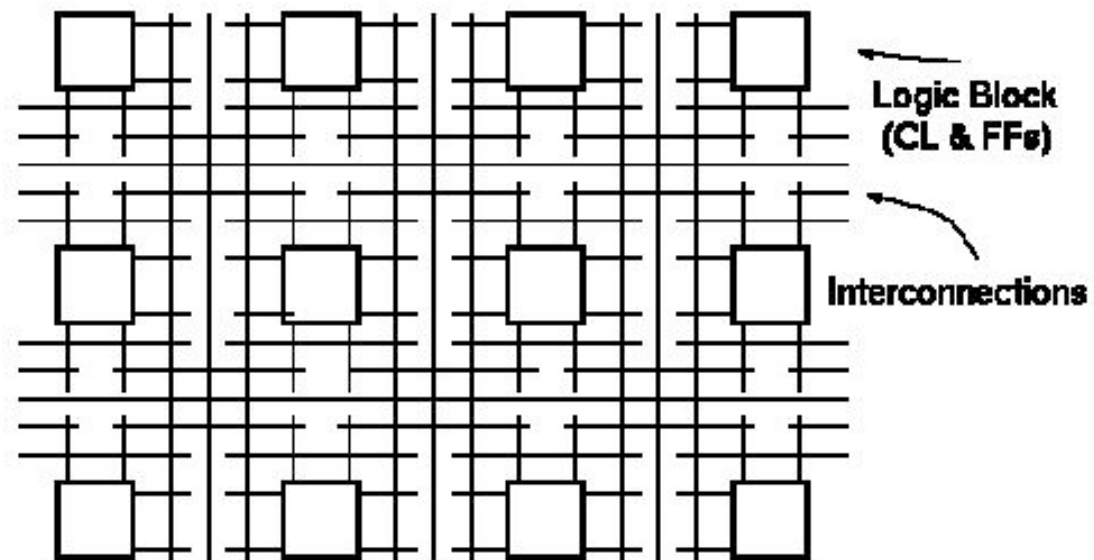
Complex Detector Electronics: FPGA's

Field Programmable Gate Arrays consist of a two dimensional array of logic blocks and flip-flops with a electrically programmable interconnections between the logic blocks.

Each **Logic block** of an FPGA can be configured to provide functionality as simple as that of transistor or as complex as that of a microprocessor. Each block can implement different combinations of combinational and sequential logic functions.

In a very simple view, operation of the FPGA includes:

1. Preprogramming the array
2. A datum/address is read in
3. The system clock is cycled
4. (changing the “state” of the machine)
5. Output may be available ...
6. Return to Step 2

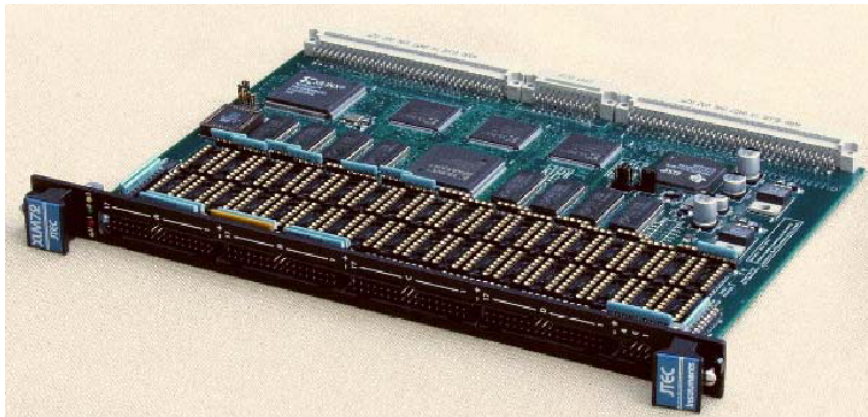


Simplified version of FPGA internal architecture:

Complex Detector Electronics: FPGA's

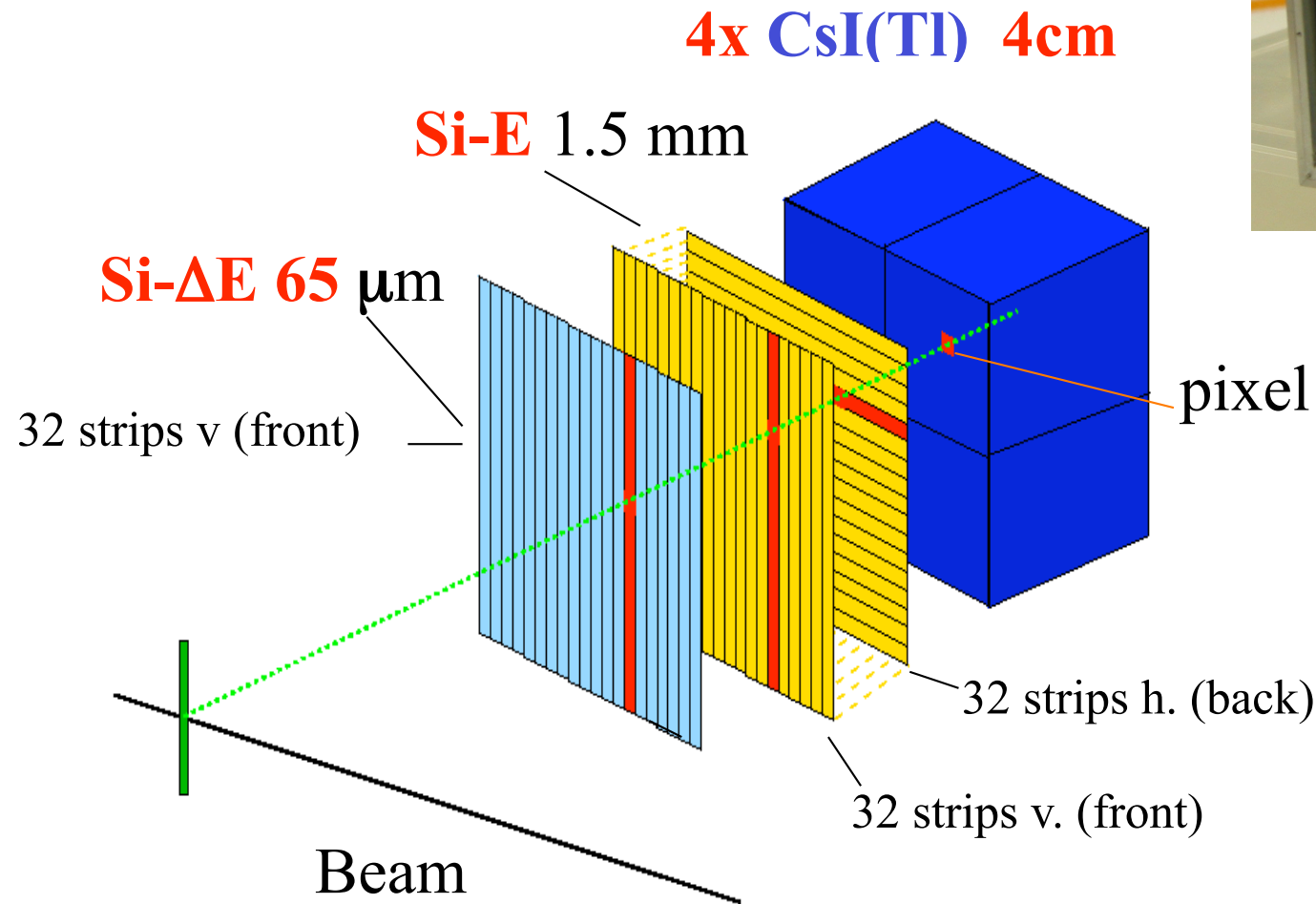
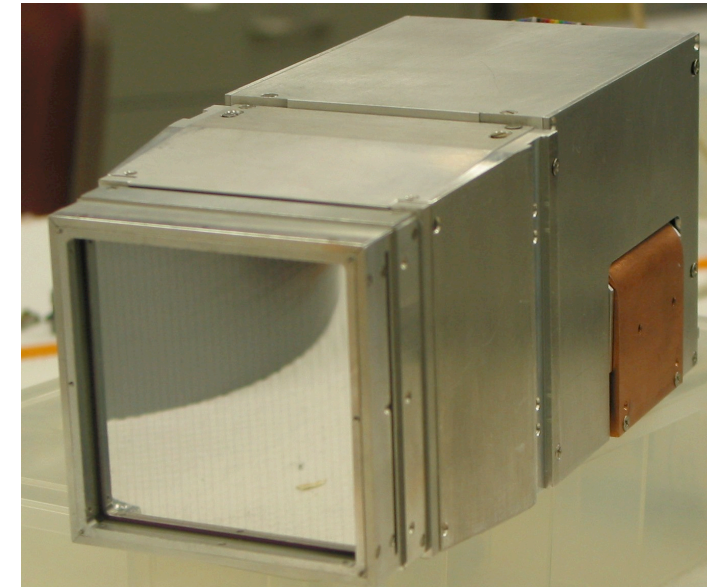
Field Programmable Gate Arrays can be found in CAMAC and VME packages ... the programming is done externally (generally with a simulation code running on a PC) and the result has to be loaded over the backplane.

LeCroy 2366 is a CAMAC-based logic module with 59 ECL lines and a Xilinx 4005 FPGA chip. Any logic that can be implemented as a synchronous (clocked) state machine may be programmed, subject only to the limitations of the size of the Xilinx gate array chip (approximately 5000 gates).



Jtec XLM72 is a universal logic VME module using a FPGA executing fast synchronous and combinatorial logic, a 900-MFlops/s floating-point Digital Signal Processor (DSP) executing complex numerical calculations, two 2-Mbyte banks of fast memory, and 72 ECL I/O ports.

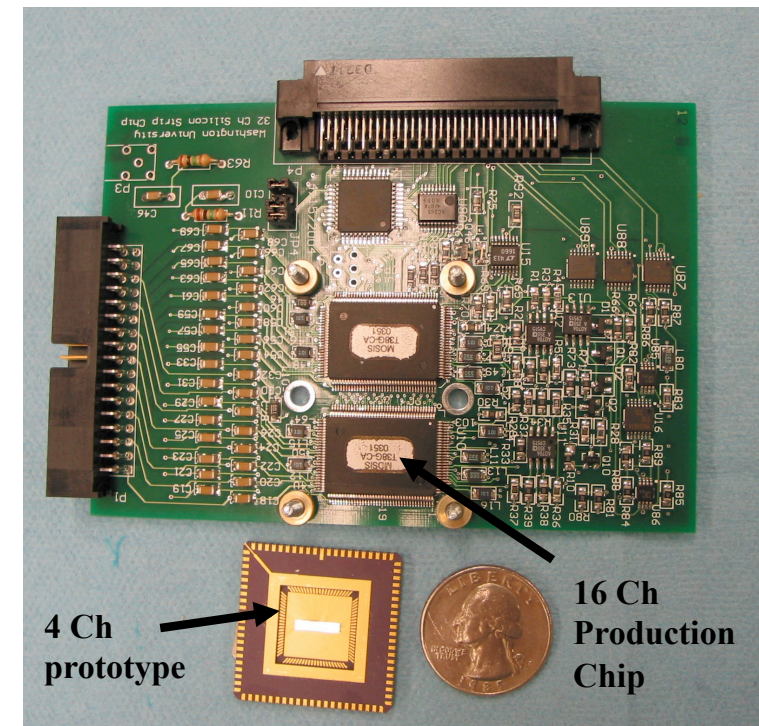
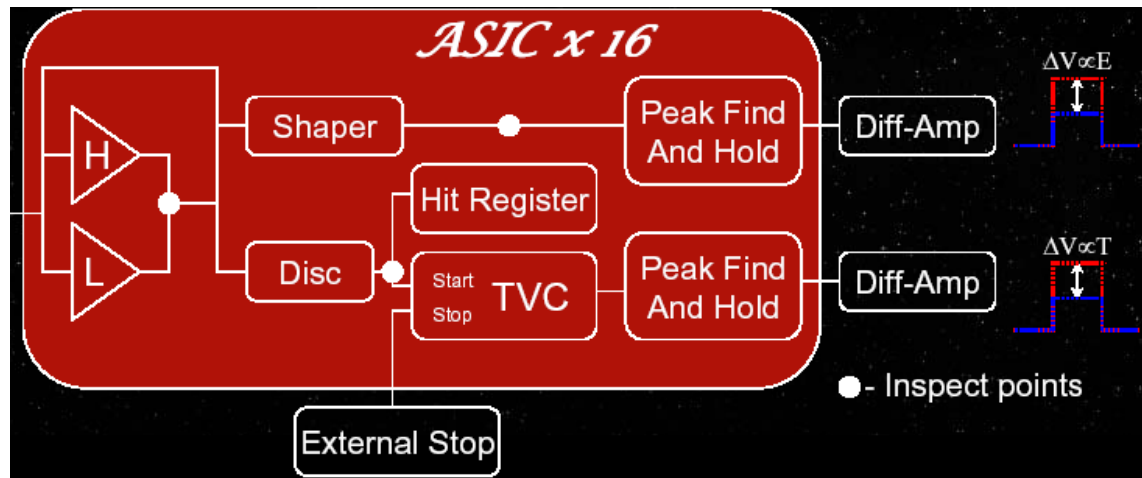
Complex Detector Electronics: HiRA Example



- 20 Telescopes
- 62.3 x 62.3 mm² Active Area
- strip pitch 1.8 mm
- 1024 Pixels per telescope

Complex Detector Electronics: HiRA ASIC

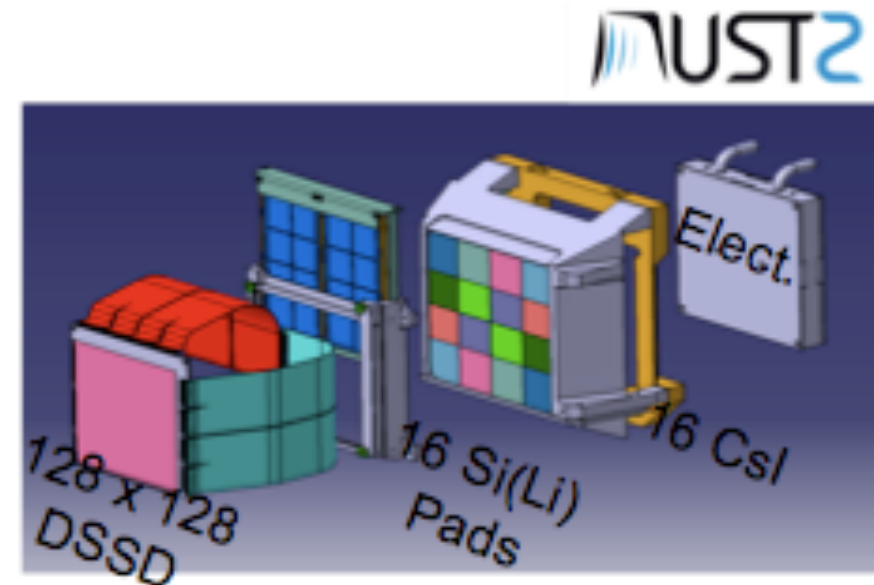
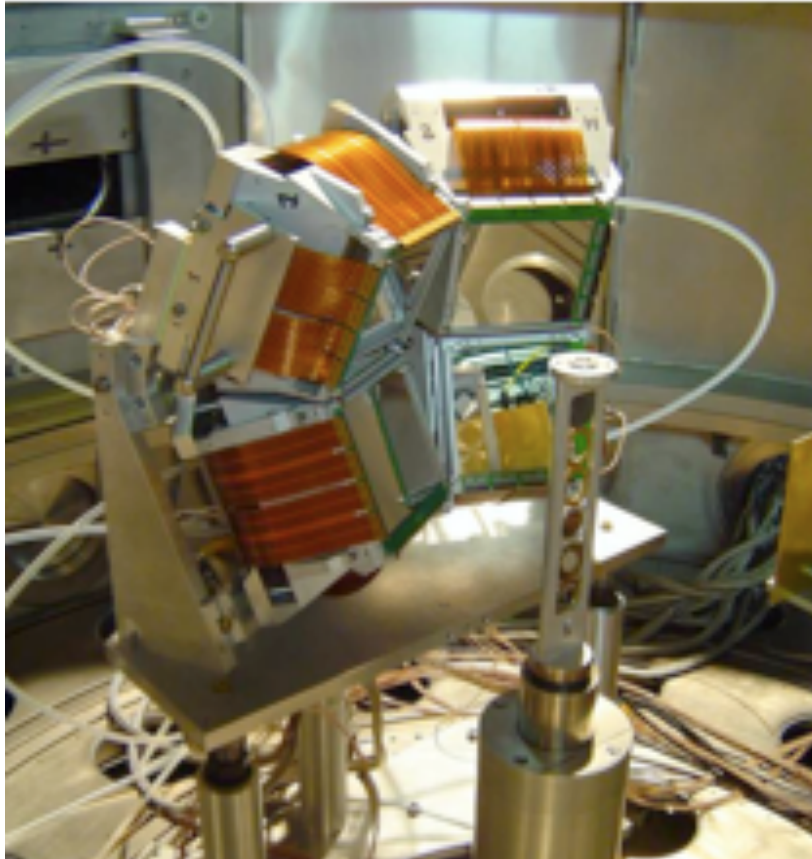
Developed at Washington University (St. Louis) and Southern Illinois University, this chip board (differential signal output) + one VME module (SIS 14-bit sampling ADC) replaces 64 pre-amp's, 32 Shapers, 32 TDCs and 32 ADCs



- Input is switchable, charge-sensitive [x1, 100 MeV(Si), x500MeV(Si)]
- Shaper x1 with 1 μ s shaping time
- Time-to-voltage signal against “stop” signal [150 ns, 1.5 μ s FS]
- Both outputs are held for external sampling by flash ADC

Test by M. Wallace showed 50 keV resolution for ^{228}Th source ...

Complex Detector Electronics: MUST2

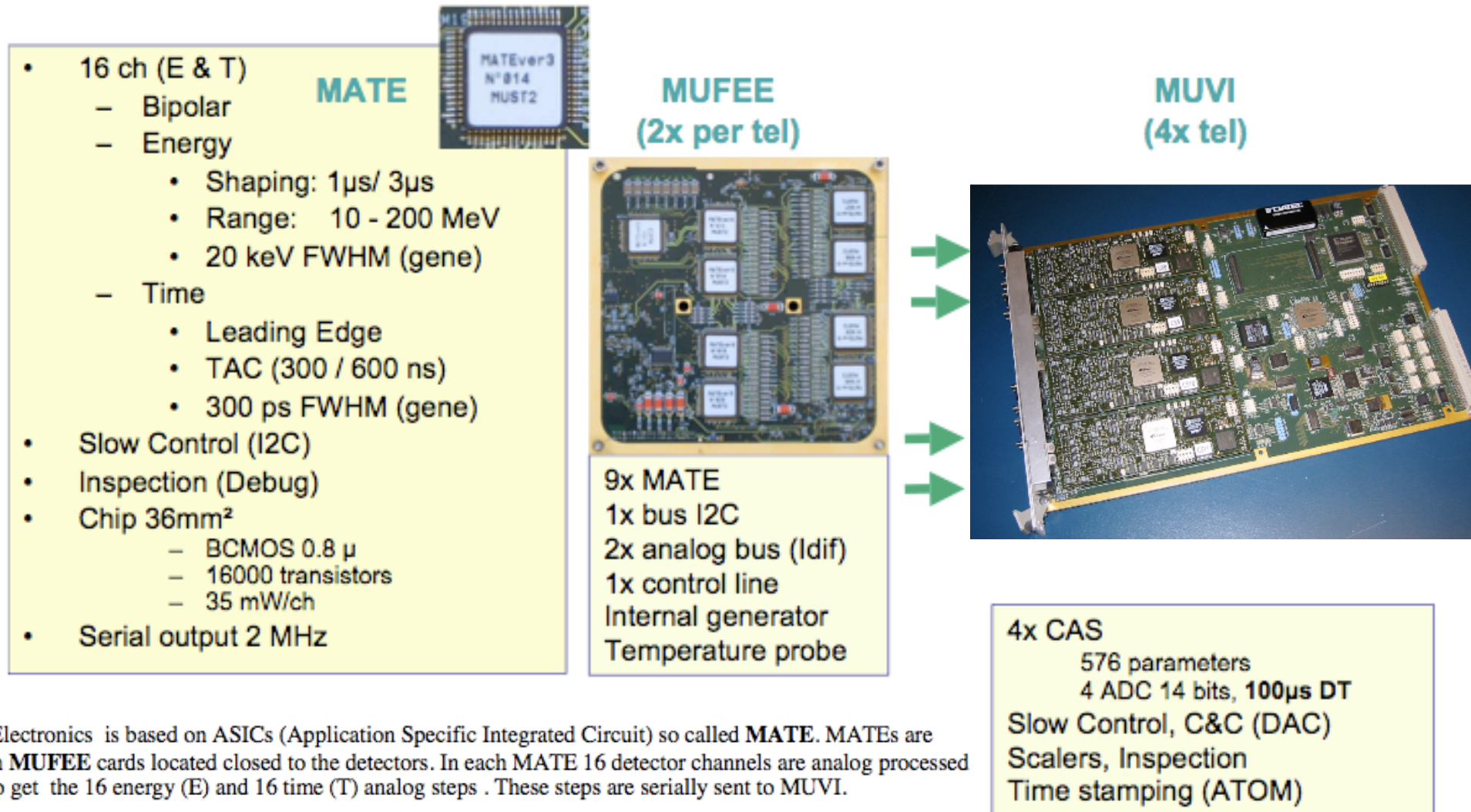


- 100 cm² area on front face
- 288 channels of Energy and Time (each)
- Si 300 μ m / Si(Li) 5mm / CsI 4cm

Project **MUST2** (**MU**r à **STrips**) is a multidetector of 10 telescopes; each telescope is made up with two X and Y plans of 128 Si tracks followed by 16 SiLi and 16 CsI. MUST2 is dedicated to the study of the light products produced from the interaction of radioactive beams with a target.

Complex Detector Electronics: MUST2

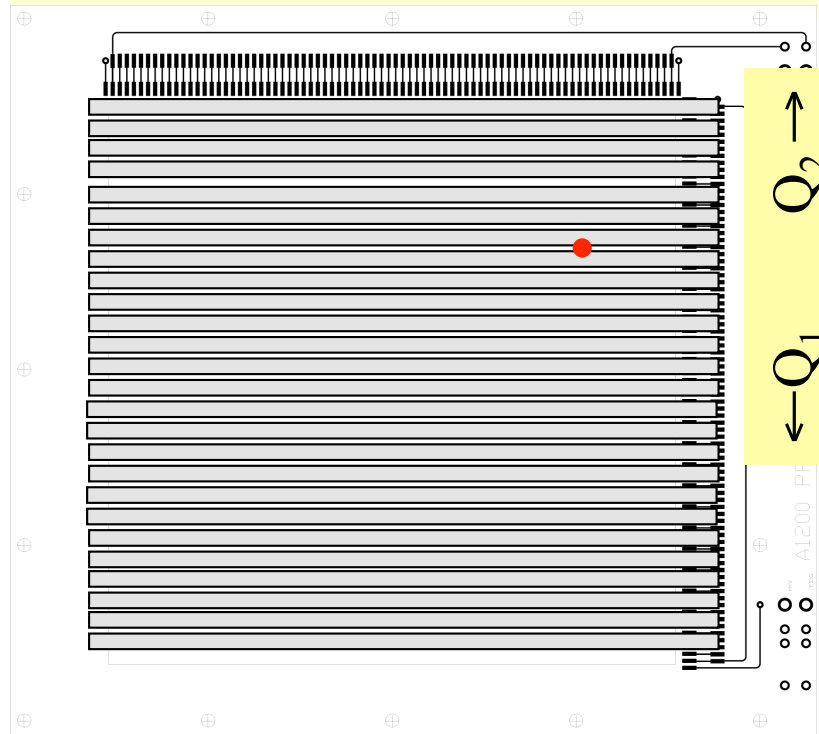
Asic solution for the Si, Si(Li) and CsI signals



MUST2 Electronics is based on ASICs (Application Specific Integrated Circuit) so called **MATE**. MATEs are housed on **MUFEE** cards located closed to the detectors. In each MATE 16 detector channels are analog processed in order to get the 16 energy (E) and 16 time (T) analog steps. These steps are serially sent to MUVI.

MUVI is a C sized VXI card in which are implemented the 14 bits analog to digital conversion, the digital processing, the physics parameters readout and the MATEs control. MUVI was specially designed in order to pay attention at the aspects of resolution, density of channel and reduction of the dead time of acquisition. It manages 4 telescopes and delivers more than 2000 E and T parameters processed in 4 **CAS** daughter cards.

Complex Detector Electronics: PPAC's ?



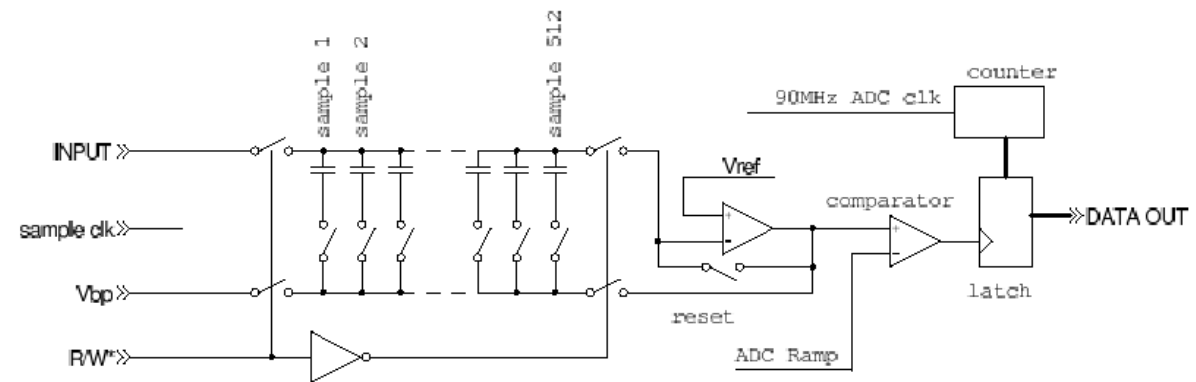
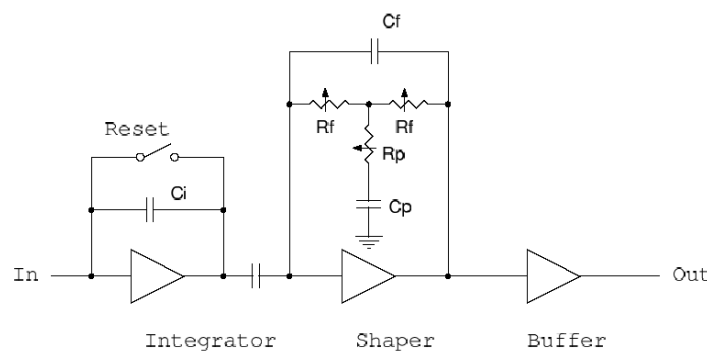
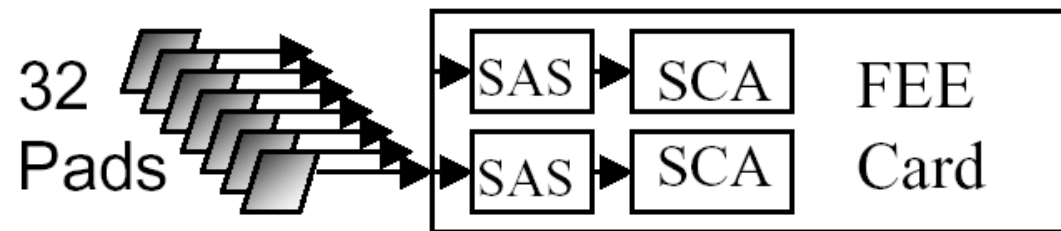
Conventional: resistor chain, two linear channels
 Problems with small signals, large size – many resistors

STAR Front-End Electronics (134k channels)

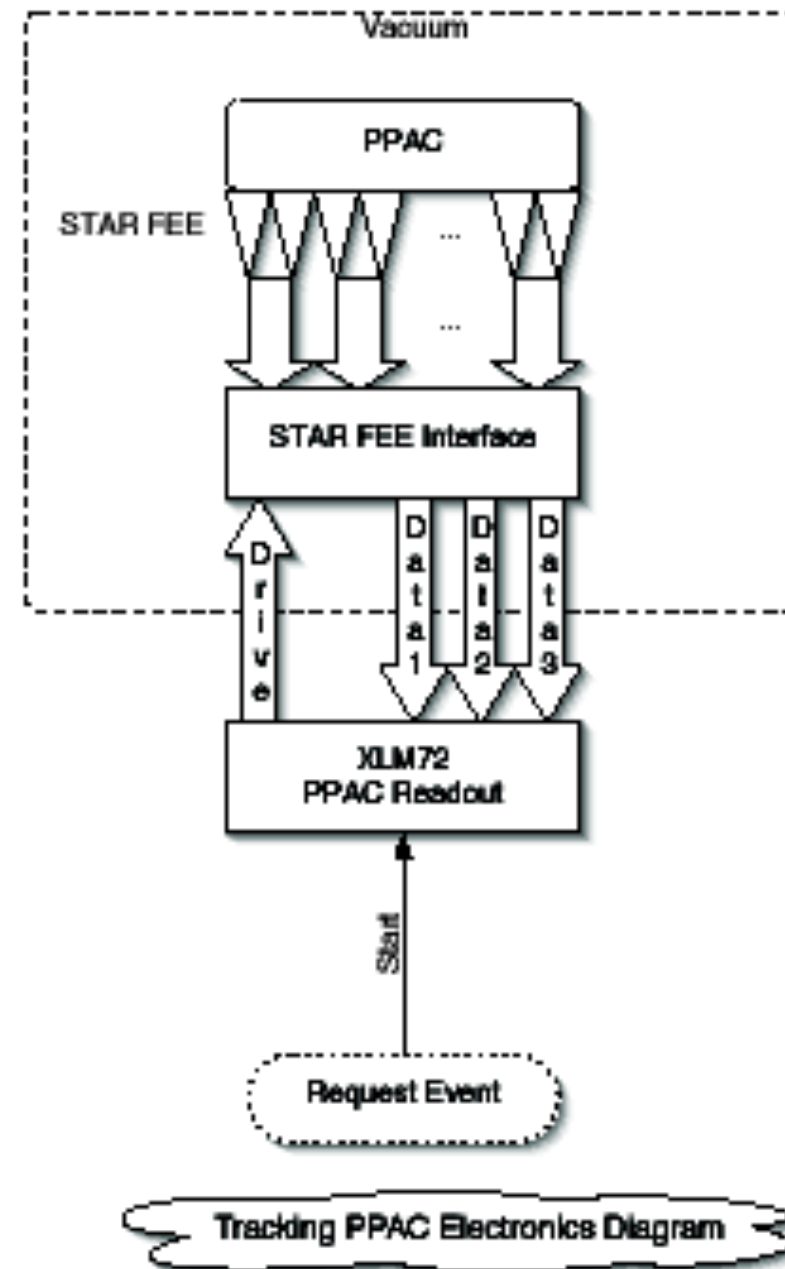
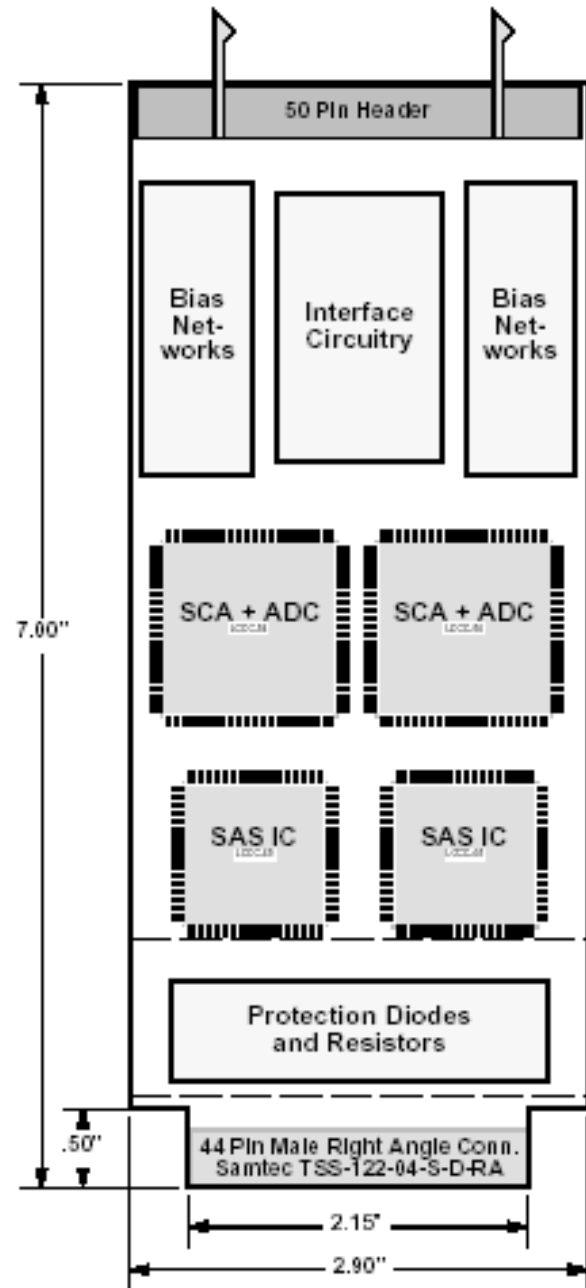
<http://arxiv.org/abs/nucl-ex/0205014>

And

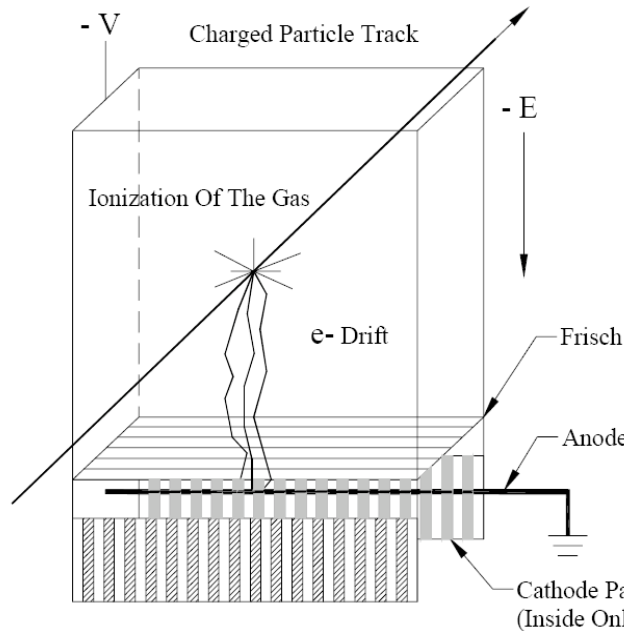
<http://www.star.bnl.gov/public/fee/fee.html>



Complex Detector Electronics: ASIC's

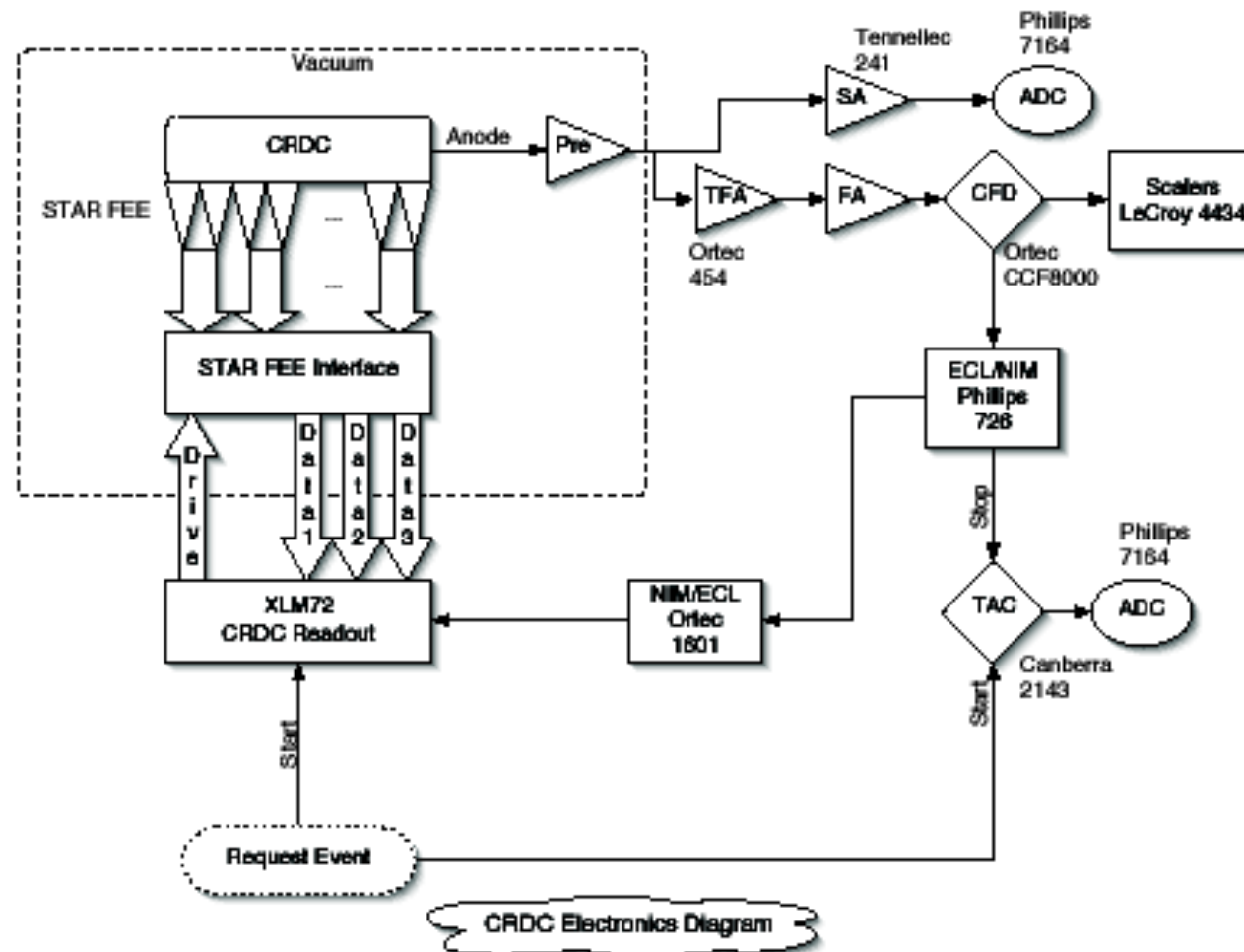


Complex Detector Electronics: CRDC Pads



(C.Freigang, MSU thesis, 2001)

Schematic diagram of Cathode-Readout Drift-Chamber used in Sweeper & S800 focal plane detectors



Chap. 18 – Data Acquisition: Question

What are the values of the full-scale voltage and the average conversion time of the (12-bit, 2mV LSB) ADC that is part of the STAR-FEE card?

