The first question to ask is "do I have more than one detector?" ..

No – simple situation, use a multichannel analyzer (MCA) described in text. In a gross overview this is an ADC connected to a digital memory that keeps track of the number of signals that fall into each bin of the ADC. Most of the hardware is associated with the display of the data in memory. (Modern devices are contained on a PCI card that plugs into a PC.)

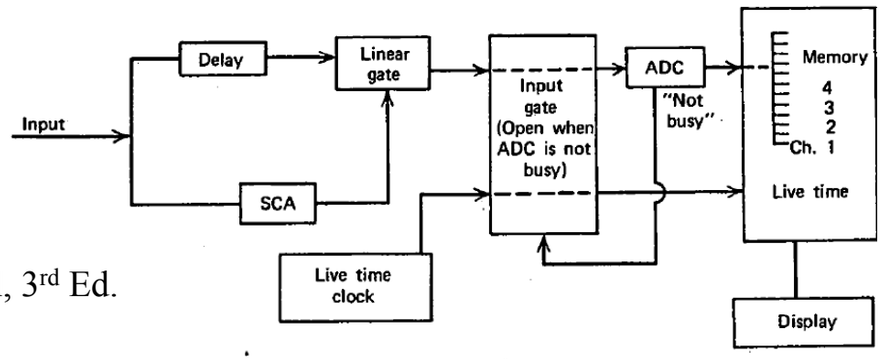


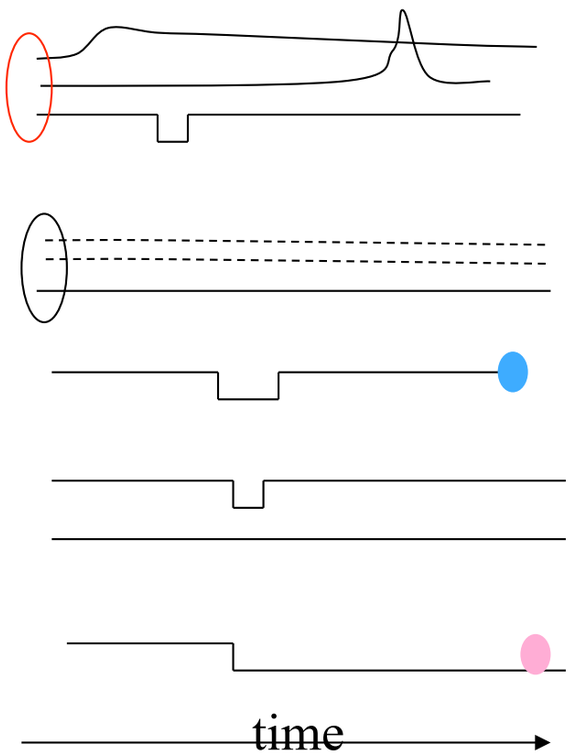
Fig. 18.7 Knoll, 3rd Ed.

Yes – more typical situation in nuclear science, generally want to retain correlations among the input signals. Up to present electronics/data recording are not fast enough to record everything (but getting closer). The experimenter has to set up the electronic logic to decide when to process and record the data. "Real Time" computing

Data Acquisition: Trigger Logic

The "trigger logic" is programmed to decide when to process and record the data.

- The output of this logic is usually called the "master gate."
- The logic usually provides "guidance" to the CPU about processing the event.
- The logic also needs to monitor the number of lost signals.
- The logic can range from individual modules to a digital logic array.
- Important logic units are AND, OR(Fan-in), LATCH, Gate&DelayGenerator



$V_i \rightarrow ADC_i$
$T_i \rightarrow TDC_i$
$\rightarrow$ ID Word$_i$
$\rightarrow$ Logic$_i$

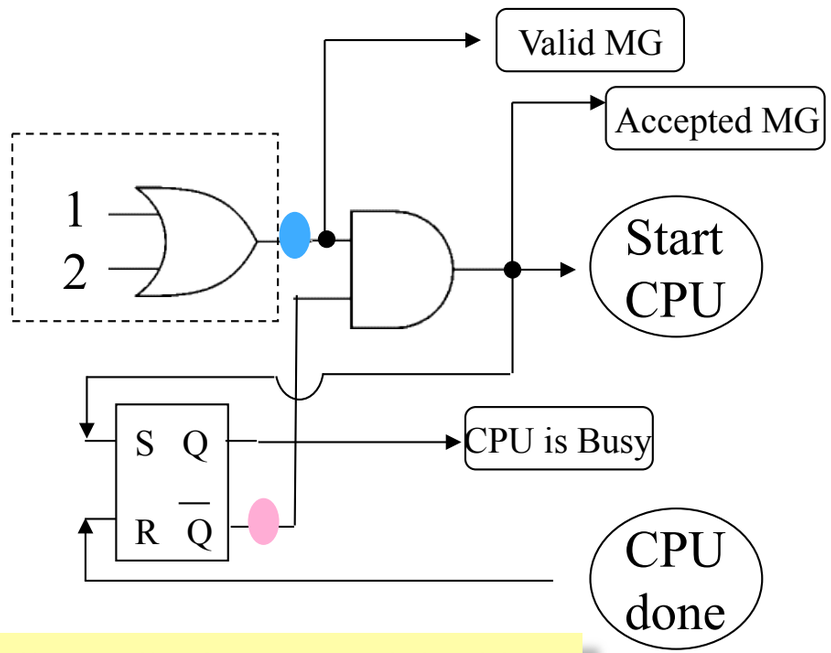
.
.

Master Gate

ID word (input-register)

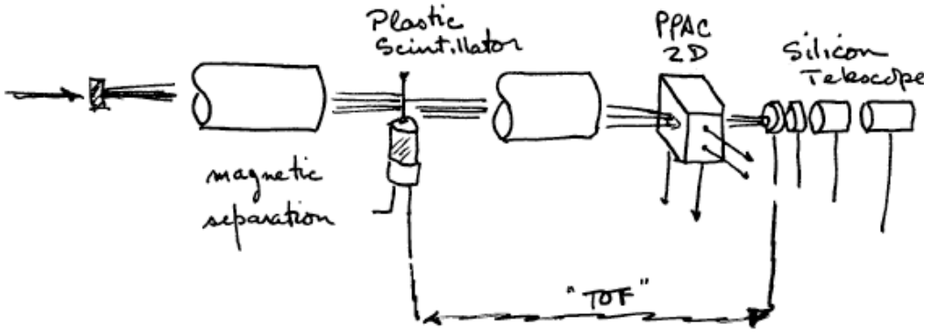
CPU not-busy

Trivial Example: 2 equivalent detectors, record when either and/or both fire.



User has to "or" all contributions to total deadtime

Data Acquisition: PID in A1900



Particle ID depends on measuring:

ToF → v or β and γ

Bρ → m β /q

ΔE → mZ²

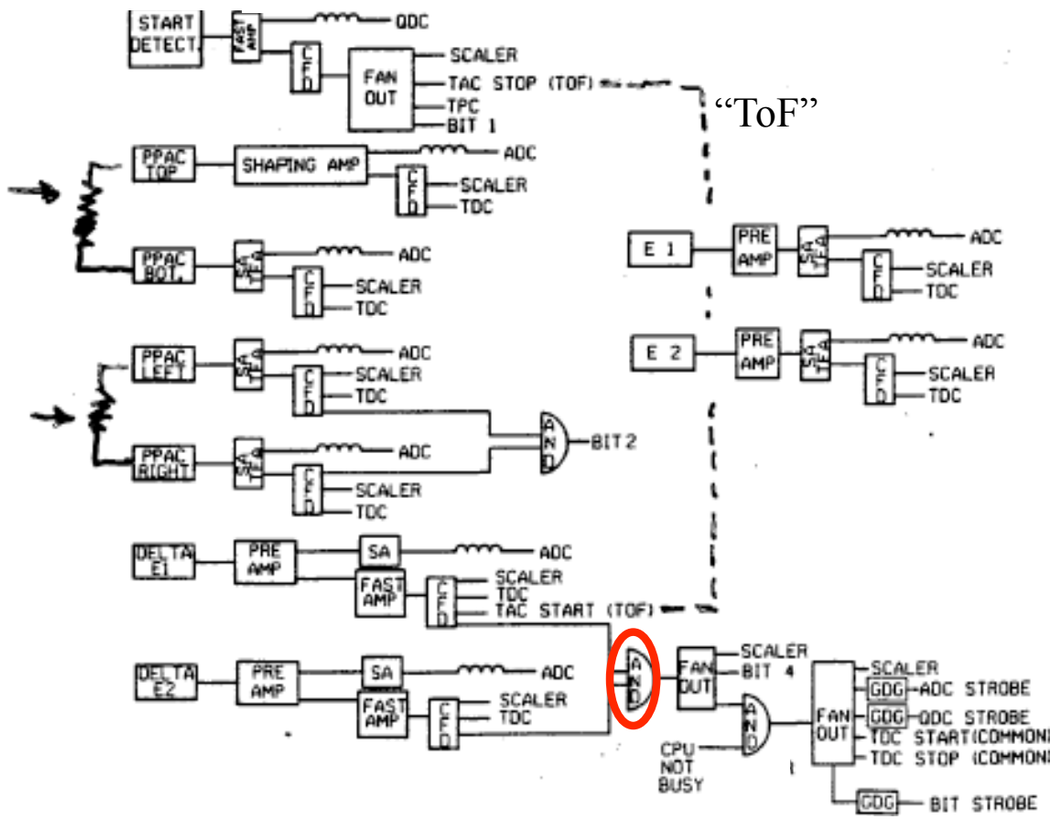
E-total → ½ mβ²

$^{A}Z^{q}$

(Z,q integer)

Notes:

Bit Register (input reg., pattern reg.)
TAC for precise ToF (stop/start)
MG is one "AND"
Scalers keep count of everything



Data Acquisition: data stream

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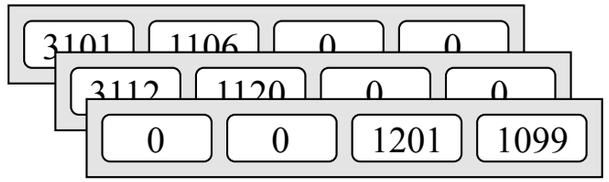
Options for Multidimensional data

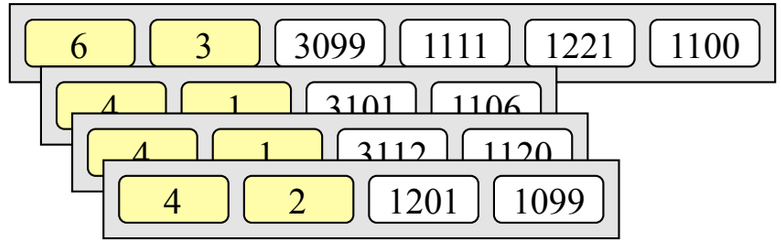
1) Record all values in order including zeros as placeholders (n-tuple)



Example of 2 detector data stream
Simple to interpret
"sparse" data (recall DSSD had 80 channels, only 2 valid)
error recovery from dropped words may be difficult

2) Record only non-zero words

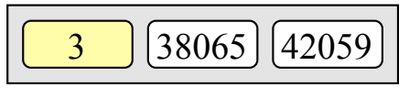
A) imbed information in data stream (plus word count, pattern register)



No gain for small experiments
Data needs to be "interpreted"
"dense" data

Problems from dropped words are localized

B) imbed information in data *words* (plus word count)



e.g. 16 bit word 4 bit ID, 12 bit data

Binary	1001 010010110001	1010 010001001011
Hexidecimal	9 4B1	A 44B
Decimal	38065	42059

Data needs more "interpretation"
High level of error checking possible

Data Acquisition: Standards

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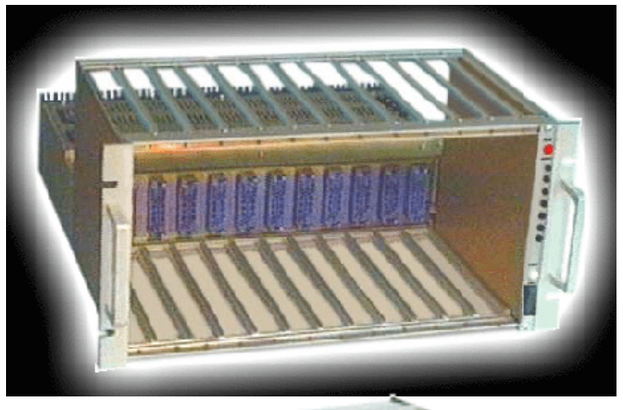
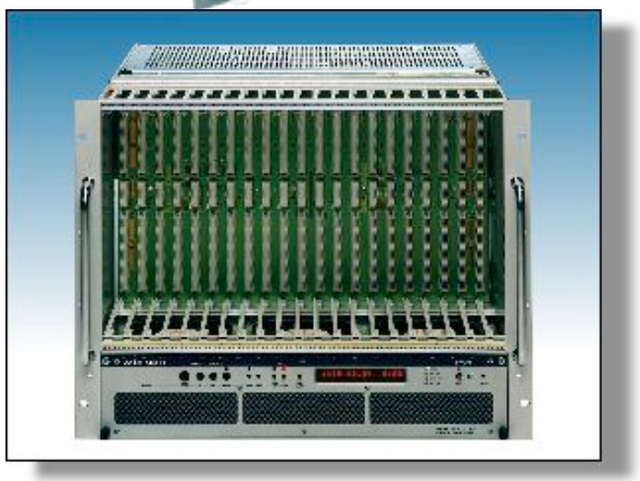


NIM (nuclear instrumentation module):
Nuclear Physics standard container/voltages/
power
Only signal lines are gate & clear (not geographic)
(not all pins on the connector block are used)

CAMAC (computer automated measurement and control):
Nuclear Physics standard container/voltages/power
Computer bus (back plane) with [86 lines]
Address lines / write / read (24b) / control lines
Bus speed 1 MHz .. Geographic: “BCNAF” “LAM”

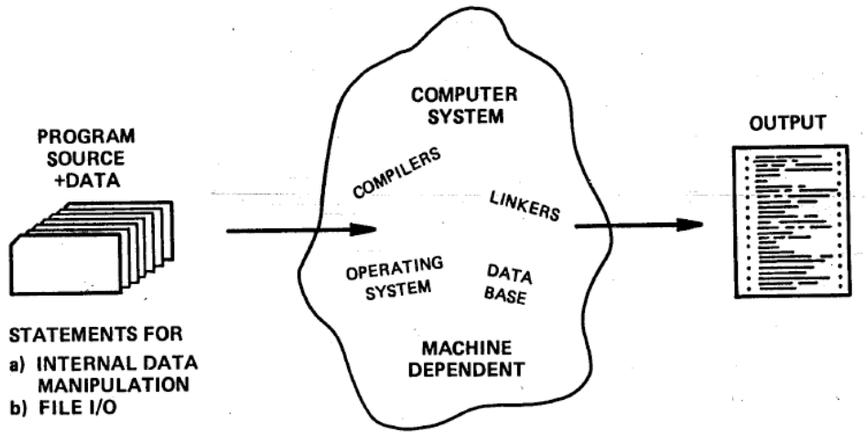


VME (Versa Module Eurocard):
industry standard container/voltages/power
Computer bus
Address lines (32b) / data lines (32b) / control lines
Bus speed 20 MHz ..
Not geographic (unless JAUX bus is used),
Memory mapped … extensions VME64, VXI

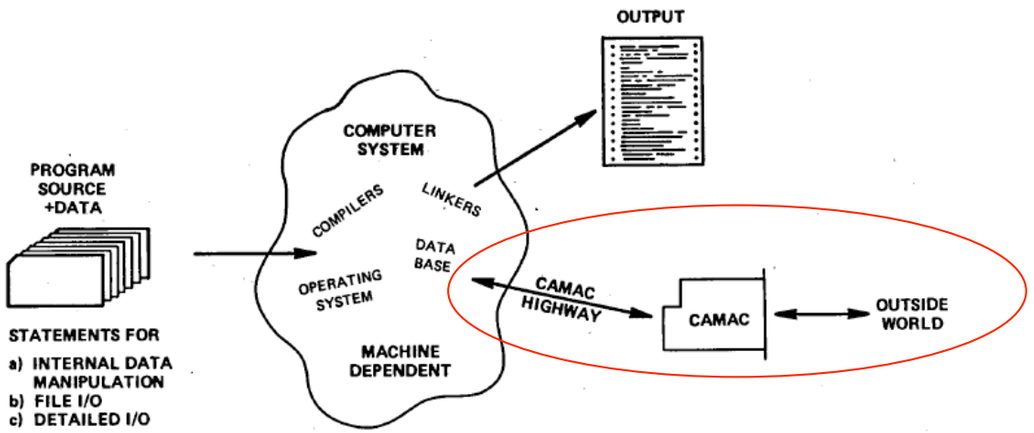
Data Acquisition: Real Time Computing

From LA-UR-82-2718 “CAMAC Primer”

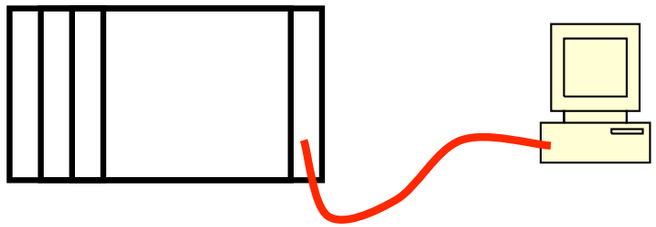
Conventional Program runs (once) in a constrained world



Real-time Program has to respond to environment



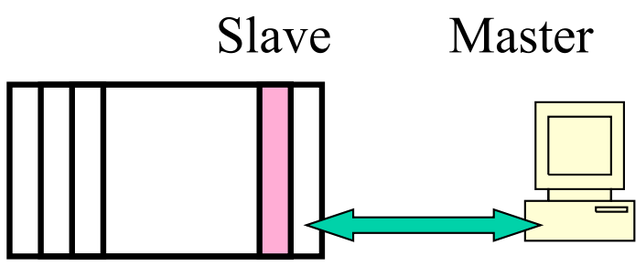
Data Acquisition: architectures – 1 –

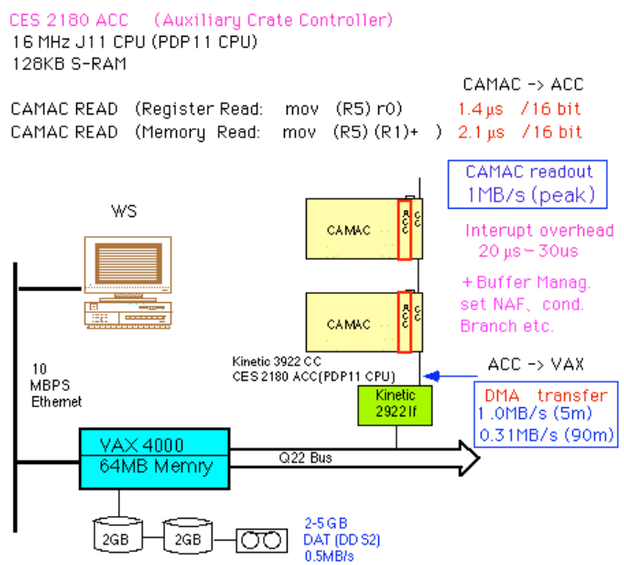


- GPIB (general purpose interface bus):
  IEEE-488 standard, 8-bit serial bus (slow)
- Serial Branch Highway: loop w/ two cables
- Parallel Branch Highway: thick cable, ~100 wires

All require appropriate adapter in CPU, slow because commands and data must travel up and down the line between computer and module through a crate controller.

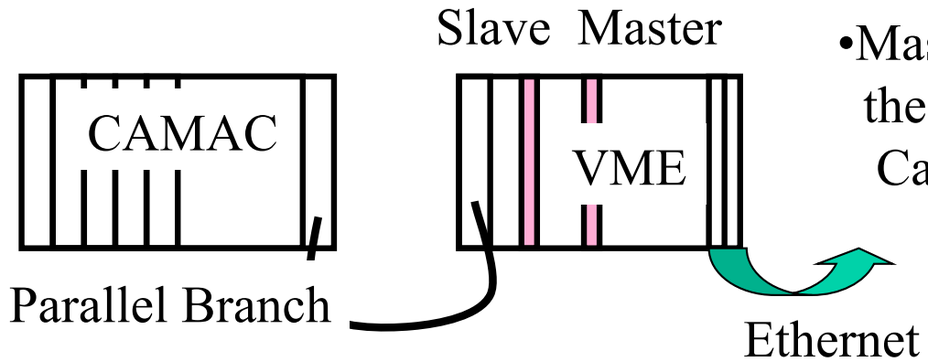
- Auxiliary crate controller: a (small) computer in the crate with a small program to collect the data into blocks and then transfer it out on command.



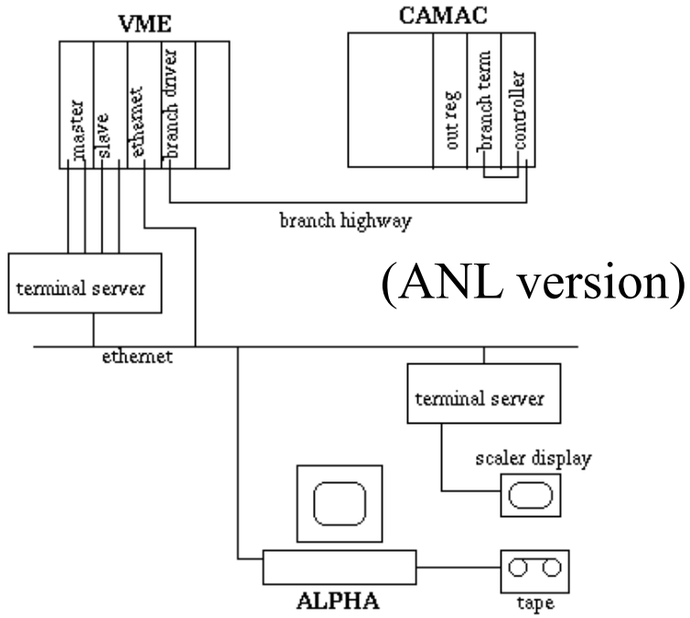


T. Ichihara et al. IEEE Transaction on Nuclear Science, 36-5 p. 1628 (1989).

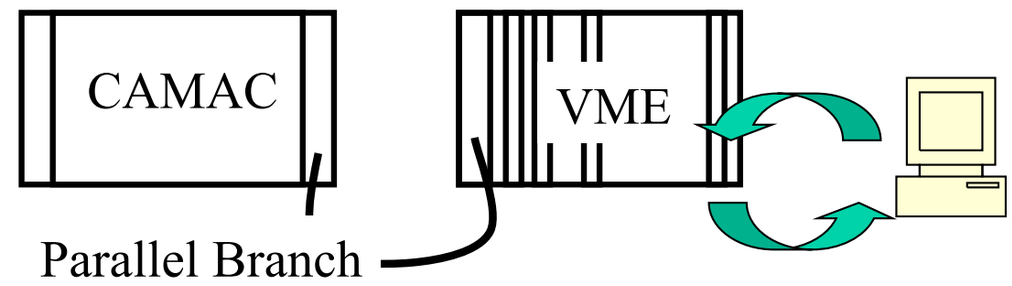
Data Acquisition: architectures – 2 –



•Master/Slave concept with VME-based CPU's
the NSCL daq system in the 1990's
Camac modules do the work



(ANL version)



Optical Fiber (PCI/VME bridge)

Back to one external CPU but connected to VME
the NSCL daq system in the 2000's
VME modules are doing the work, camac can be dropped

Chap. 18 – Data Acquisition: Question

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The present NSCL data acquisition system relies on successive approximation ADC's that require approximately 10μs to complete the conversion of all analog signals into digital words. The ACS's reside in CAMAC crates serviced by a code running in a LINUX computer (through PCI/VME and then VME/CAMAC interfaces). The time to store a data word from the module in the computer memory is approximately 3μs, assume other overhead times are negligible. (a) Estimate the deadtime per event if this system is used to readout an experiment that has ten parameters (ten data words). (b) Estimate the fractional deadtime if this ten-parameter experiment is running at the rate of 200 events/sec. (c) At what event rate will the system reach a fractional deadtime of 0.50 (at ten words/event)?
[Final Exam Question, F/2oo2]