# Chap 18a – A/Q/T to Digital

**Final step in pulse processing is to convert the analog signal into a digital word.**

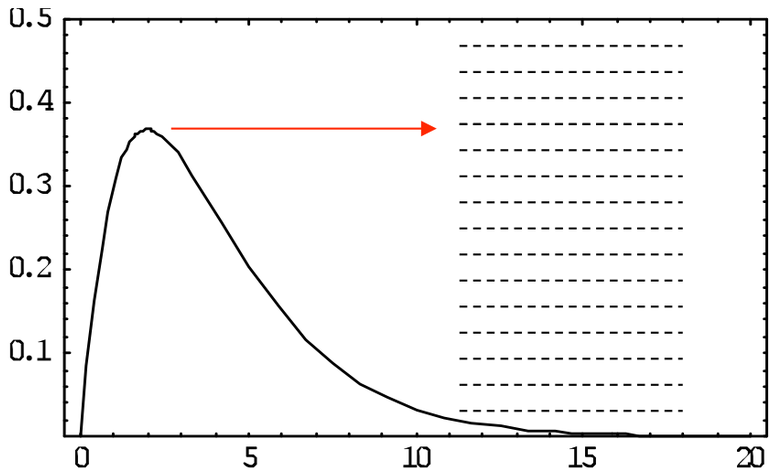
The input signal can be a voltage, charge or time difference and is compared to a reference voltage or charge by a variety of techniques. The choice of comparison circuit (procedure) generally determines:

Resolution, Non-linearity (integral and differential), and Conversion time

Resolution: the resolution of an ADC is specified in terms of both the (voltage) range and the digital range (number of bits).

The voltage associated with the least significant bit (LSB) is $(V_{max} - V_{min}) / 2^N$

Perfect device sorts the data into $2^N$ bins of equal width = 1 LSB




Example: $\Delta V = 0.5$ V

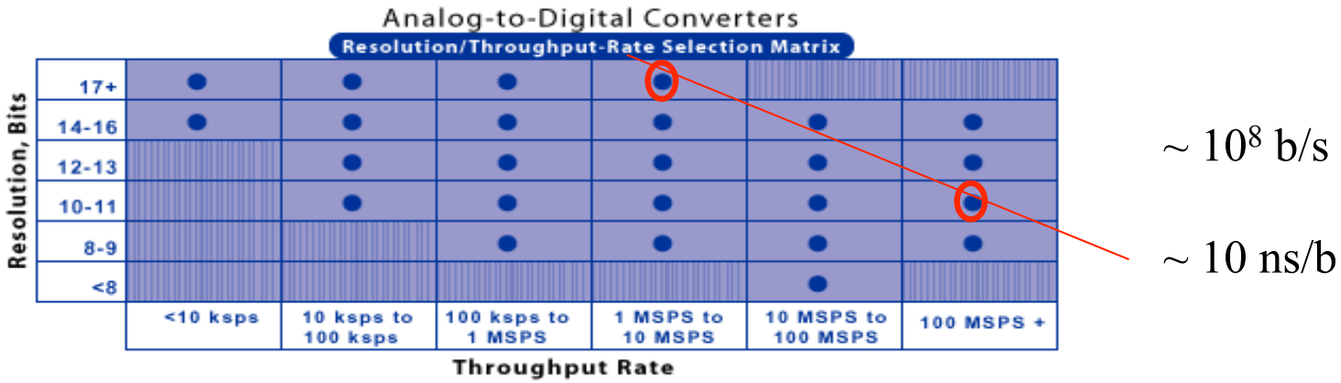
$N=4$, $2^N=16$ $V_{LSB} = 0.03125$

Peak in bin #:

Decimal: 12 binary: 1100, Hex: C

# Analog to Digital: conversion time

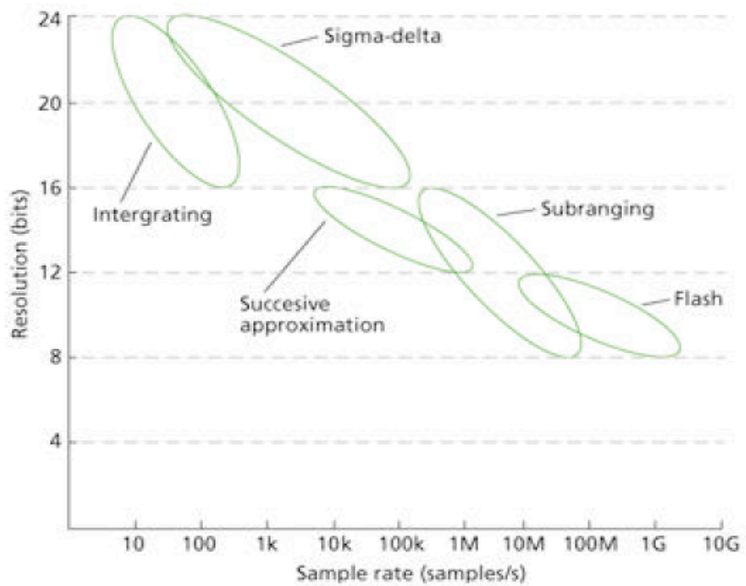
The input circuit can scale the input voltage range, the number of bins and the conversion time (or input rate limit) are linked.
The following table is from the manufacturer *Analog Devices (www.analog.com)*




~ $10^8$ b/s

~ 10 ns/b

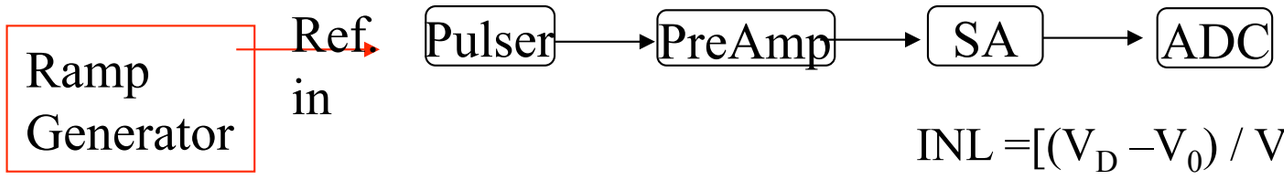
The algorithm used to convert the signal is correlated with the speed and resolution. Most modern devices are used in a nearly continuous mode, rather than in a pulse processing mode.



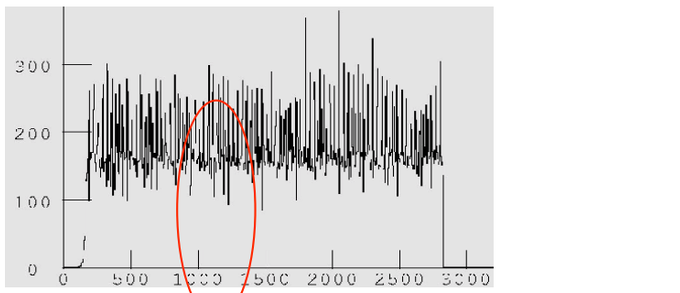

Typical nuclear physics pulsed device 12b /10 μs ~ $10^7$ b/s

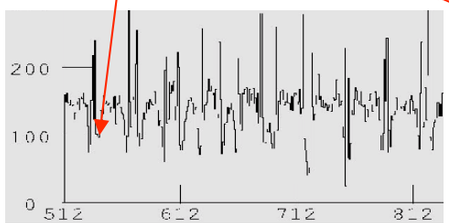
# Analog to Digital: Linearity

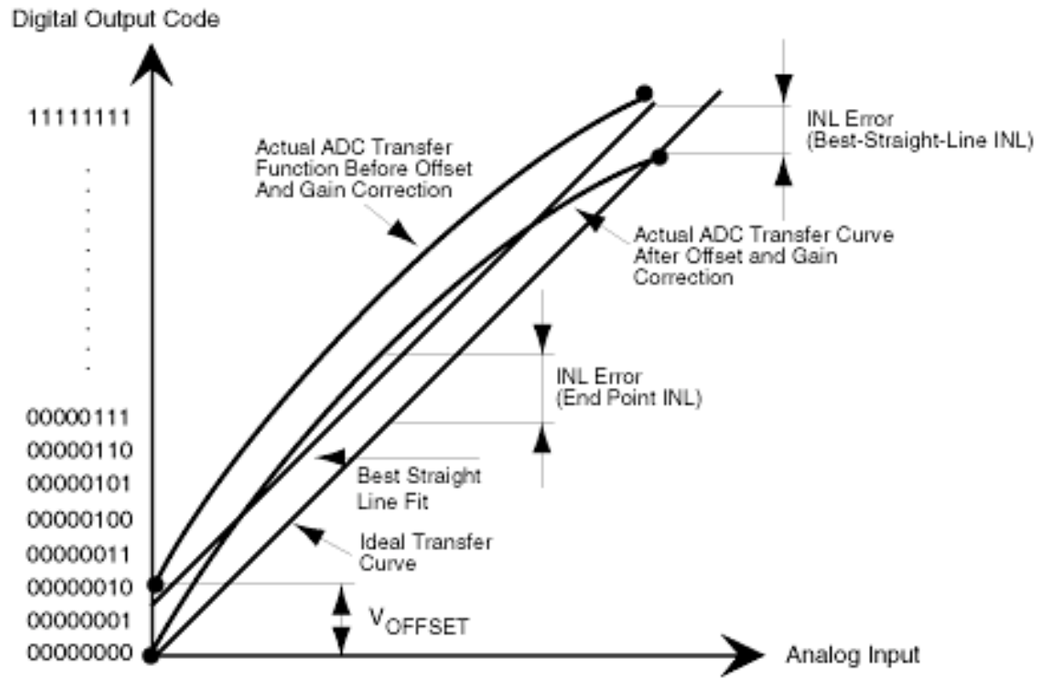
The devices are expected to be linear – thus the small deviations are quoted in terms of the integral and differential non-linearity (INL & DNL).




$$INL = [(V_D - V_0) / V_{LSB}] - D$$



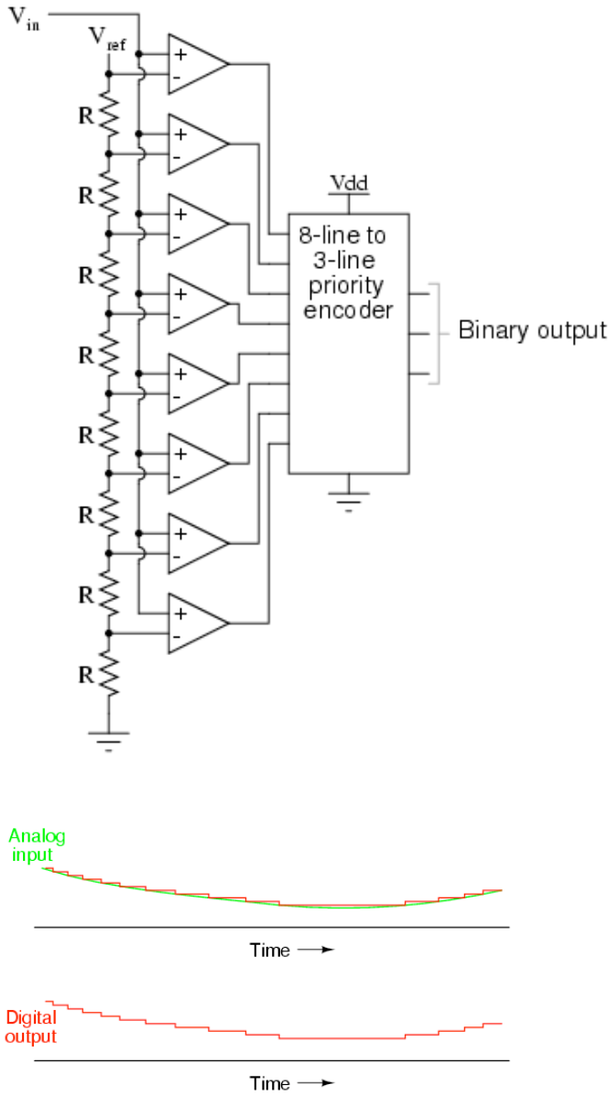




See alternate version:

Fig. 18.6 Knoll, 3rd Ed.

$$DNL = (\Delta V_i / V_{LSB}) - 1$$

# Analog to Digital: Flash ADC




A Flash ADC is the fastest device: the input is compared to a set of reference voltages simultaneously.
Uniform conversion time.
Hardware intensive: $2^N$ comparators
Nonlinear: resistor chain & comparators

Use in nuclear physics limited to digital signal recording

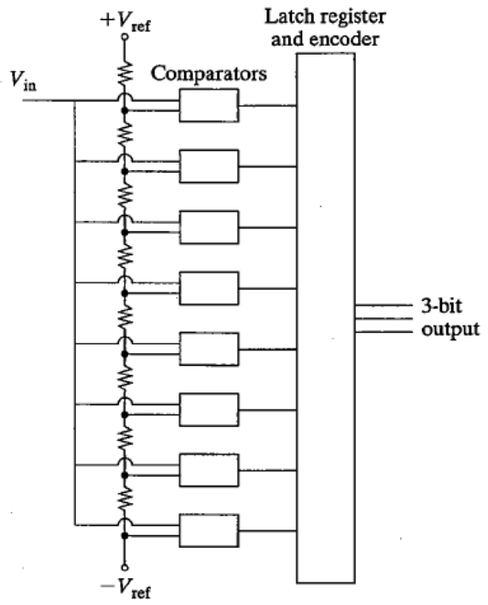
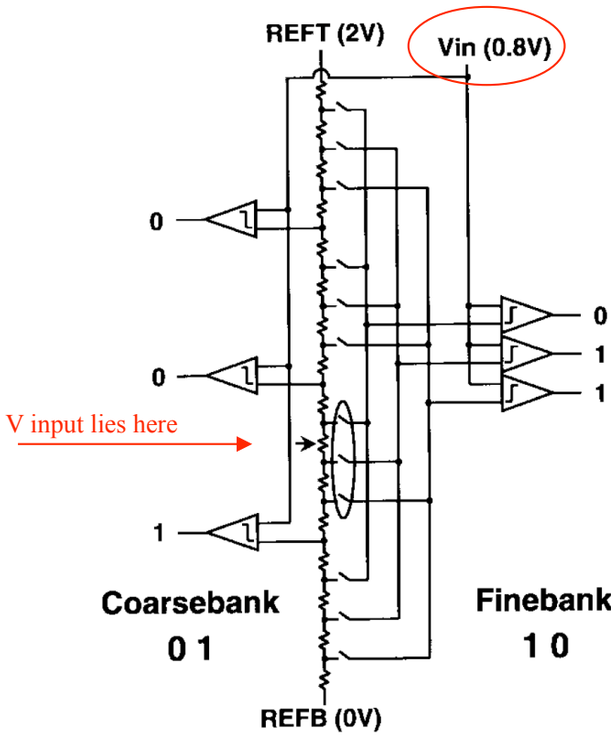



Fig. 17.31 Knoll, 3rd Ed.

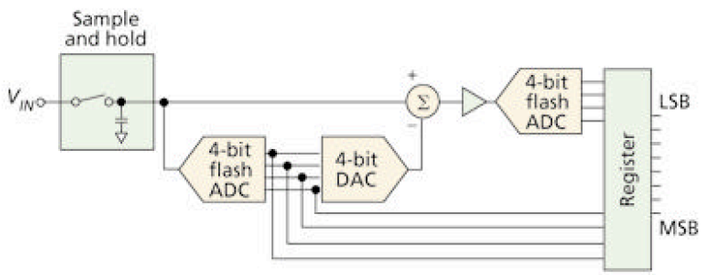
# Analog to Digital: sub-ranging ADC




A sub-ranging ADC compares the input signal to the voltage on a resistor chain using several banks of comparators in sequence.

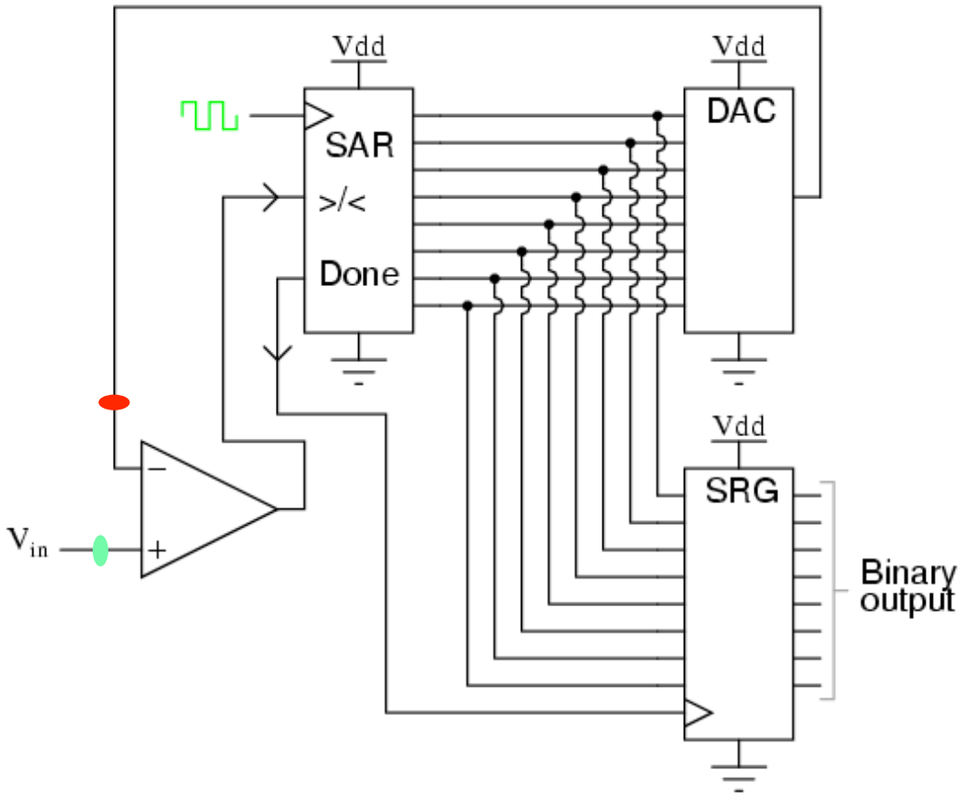
Uniform conversion time.
Hardware requires switching banks several comparators
Linearity & Resolution limited by resistor chain and comparators

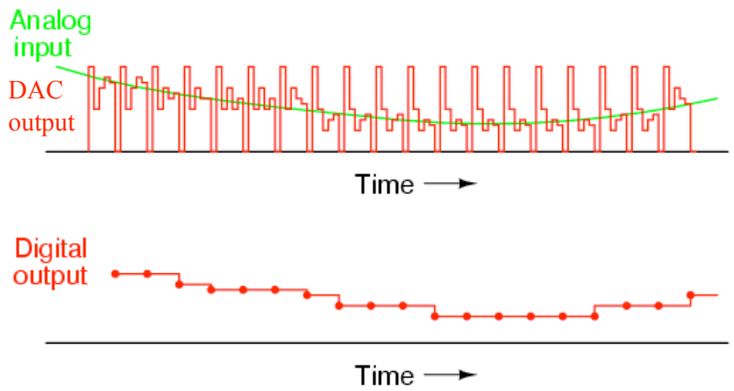
Example:
0.8 V (2V range) → 40% (FS is $2^4$)
0.4 * 16 = 6.4 , expect $6_{decimal} = 0110_{binary}$




Alternate device determines the upper range and then subtracts it away with a DAC signal … 15 comparators in each flash ADC to process the signal compared to $2^8$ comparators in an 8-bit flash ADC.

# Analog to Digital: successive approximation



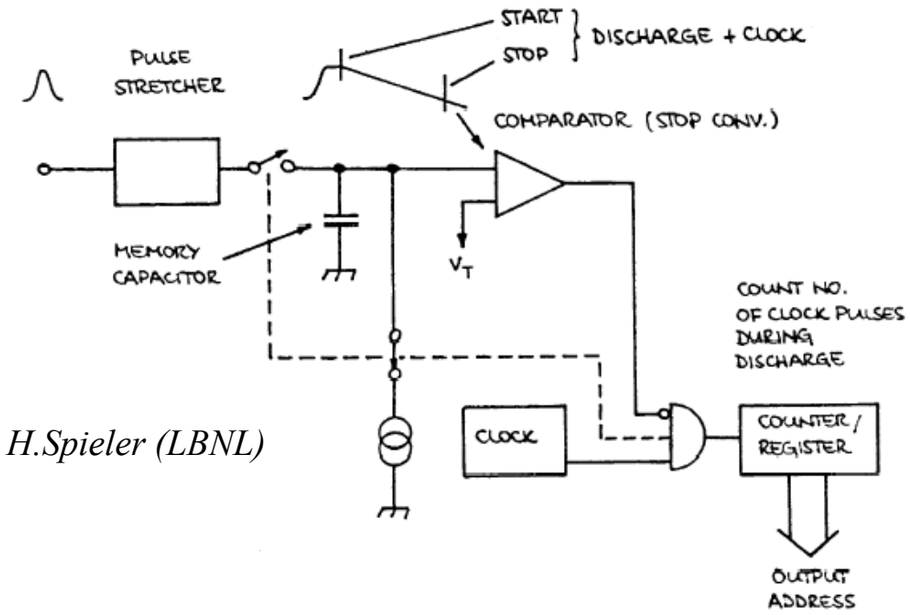




A successive-approximation ADC compares the input signal to a digitally generated signal starting at the midpoint of the range.

Uniform conversion time.
Hardware requires accurate DAC
Linearity: one comparitor but DAC
Resolution limited by DAC

Very common in nuclear physics but not for the highest resolution systems.

# Analog to Digital: Wilkinson Ramp ADC

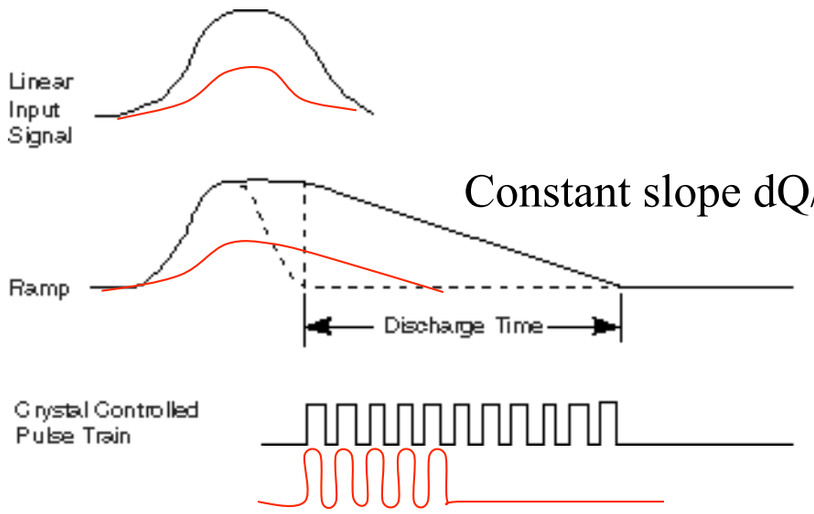



*H.Spieler (LBNL)*

The input signal is stored as a charge on a capacitor that is discharged by a constant current source with a clock (100 up to 400 MHz )

Variable conversion time.
Linearity: one comparitor but stretcher
Input rate limited by clock rate

Highest resolution devices in nuclear physics, used for Ge detectors.



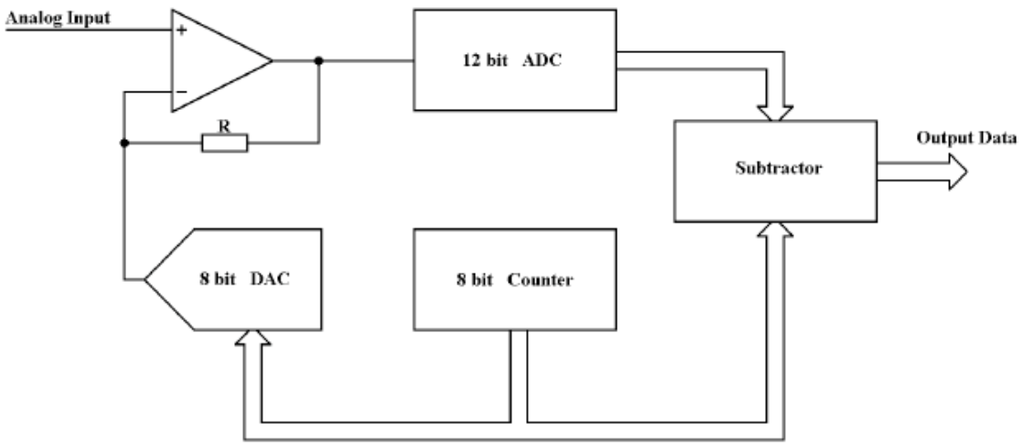

Constant slope dQ/dt

8192 /400 MHz ~ 20 μs

# Analog to Digital: the Gatti Register

The highest resolution ADC's generally over-sample the signal using a technique based on the "Gatti Register" or sliding-scale register (Cottini, Gatti, & Svelto NIM 24 (1963)241) to improve the differential non-linearity by averaging the response of the ADC. There is no free lunch, the averaging results in a loss of some dynamic range.

One example of many variations:




*R.Bassini, et al. (InFN-Milano)*

See alternate version:

Fig. 18.10 Knoll, 3rd Ed.

Example: $2^{12} = 4096$ channels

$2^{8} = 256$ channels

Values in range 3840-4096 not valid!

- The counter contains a random number and generates a voltage that is added to the input voltage.
- The analog signal is converted to a large number but the value of the counter is then subtracted.
- The counter is incremented before the next pulse.

The net effect for many pulses is to smear out the DNL.

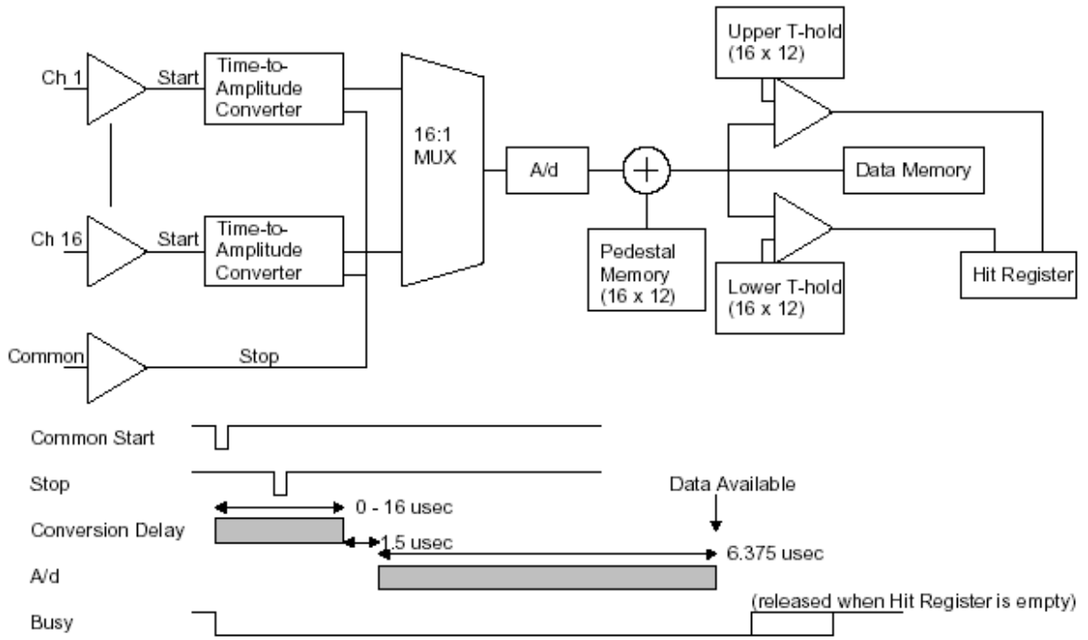
N.B. The voltage step of each bit in the DAC must be exactly equal to the step size (LSB) in the ADC.

# Analog to Digital: time to digital

Time differences are recorded in two ways:

•Creation of an amplitude signal from the time difference followed by a "normal" ADC

Phillips Scientific 7186




•Counting clock pulses between start/stop signals – generally limited to Dt =1ns or lower resolution, can read multiple hits before & after start (with appropriate logic)

# Chap. 18 – Analog to Digital: question

MICHIGAN STATE UNIVERSITY

Problem 18.11 – The following data is part of a gamma-ray pulse height spectrum. It can be assumed that the data consist of a constant background plus a Gaussian peak.

a) Plot the data, estimate the constant background level, find the net number of counts, estimate the centroid and FWHM.

b) Fit the data with a Gaussian function …

Problem 18.10 – Plot the second derivative of .. (the data).