Week 14: Chap. 18c High-D Detectors

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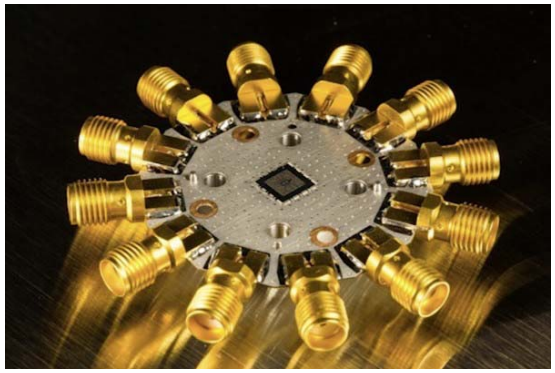
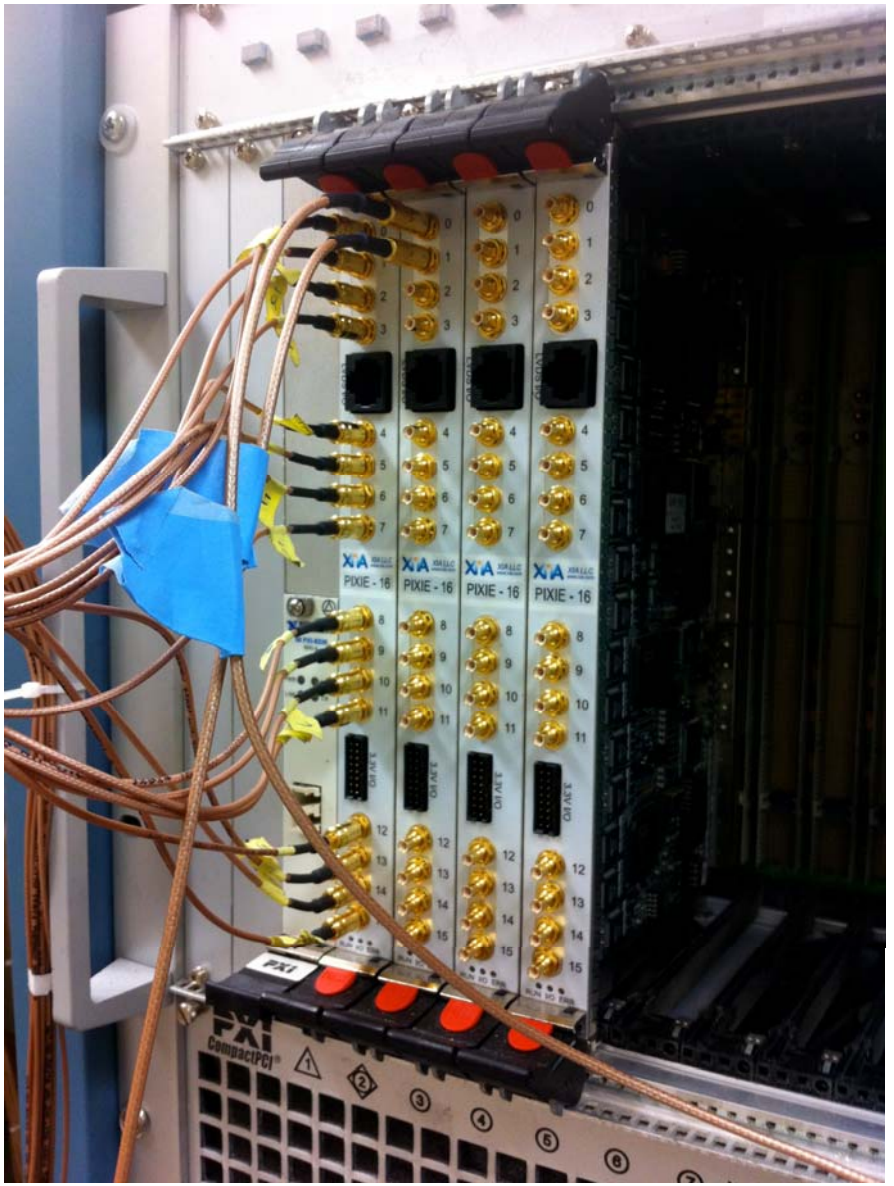
Multidimensional DAQ

High Dimensional Detector Systems
-- FPGA's
-- Digital DAQ
-- ASICs
--- HiRA ASIC
--- MUST ASIC
--- STAR FEE card

Miscellaneous Detectors





XIA PIXE-16's

Complex Detector Electronics: FPGA's & ASIC's

Complex systems and experiments with very high channel counts need to process a large number of signals and make logical decisions rapidly. Options for "electronic decision makers" include: a microprocessor (in CAMAC or VME), a field-programmable gate-array (FPGA), or an application-specific integrated-circuit (ASIC).

http://www.tutorial-reports.com/computer-science

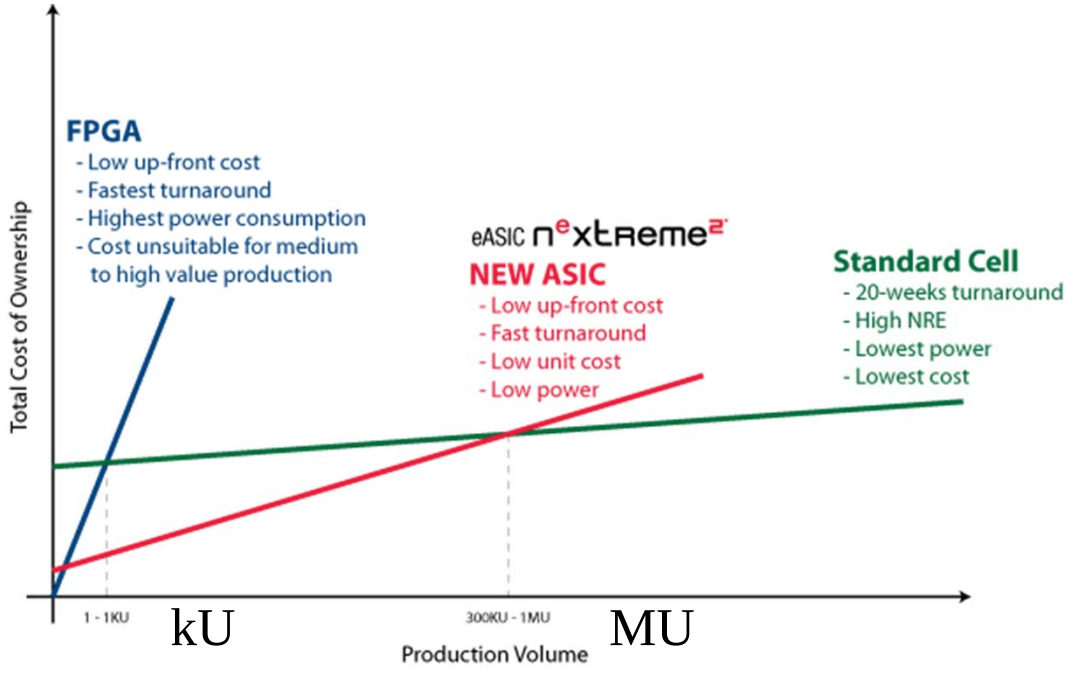
	performance	NREs	Unit cost	TTM
High	ASIC	ASIC	FPGA	ASIC
	FPGA	FPGA	MICRO	FPGA
Low	MICRO	MICRO	ASIC	MICRO

ASIC = custom IC, MICRO = microprocessor

FPGA's ... the manufacturer
http://www.xilinx.com/

ASIC's … a course:
http://www.csit-sun.pub.ro/resources/asic/CH01.pdf

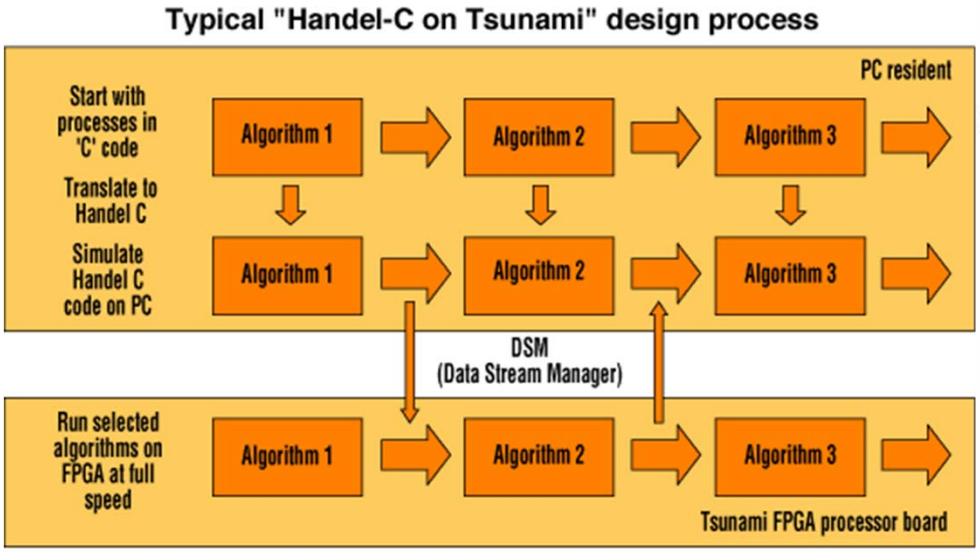
NRE's – non-recurring eng. costs
TTM – time to market



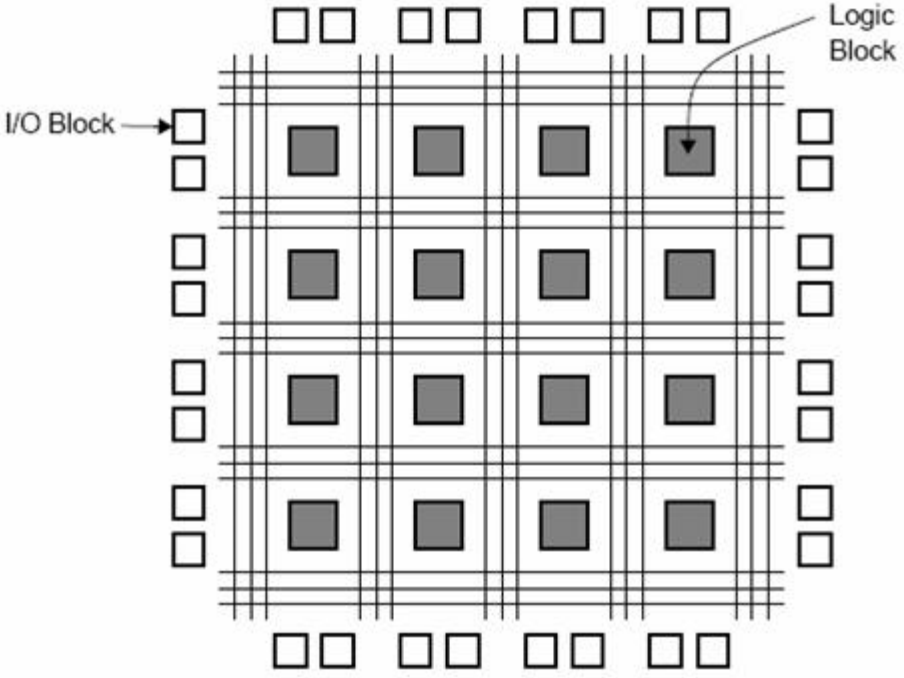
Complex Detector Electronics: FPGA's

Field **P**rogrammable **G**ate **A**rrays consist of a two dimensional array of logic blocks and flip-flops with electrically programmable interconnections between the logic blocks. FPGA companies put their effort into the FPGA architecture and the software, where it is much easier to make a profit than building chips.

Each **Logic block** of an FPGA can be configured to provide functionality as simple as that of transistor (switch) or as complex as that of a microprocessor. Each block can implement different combinations of combinational and sequential logic functions.



Accelerating a C-based algorithm involves translating the code to Handel-C, simulating the Handle-C design on a PC, and then running the design on an FPGA processor.



http://www.tutorial-reports.com/computer-science

Complex Detector Electronics: FPGA's

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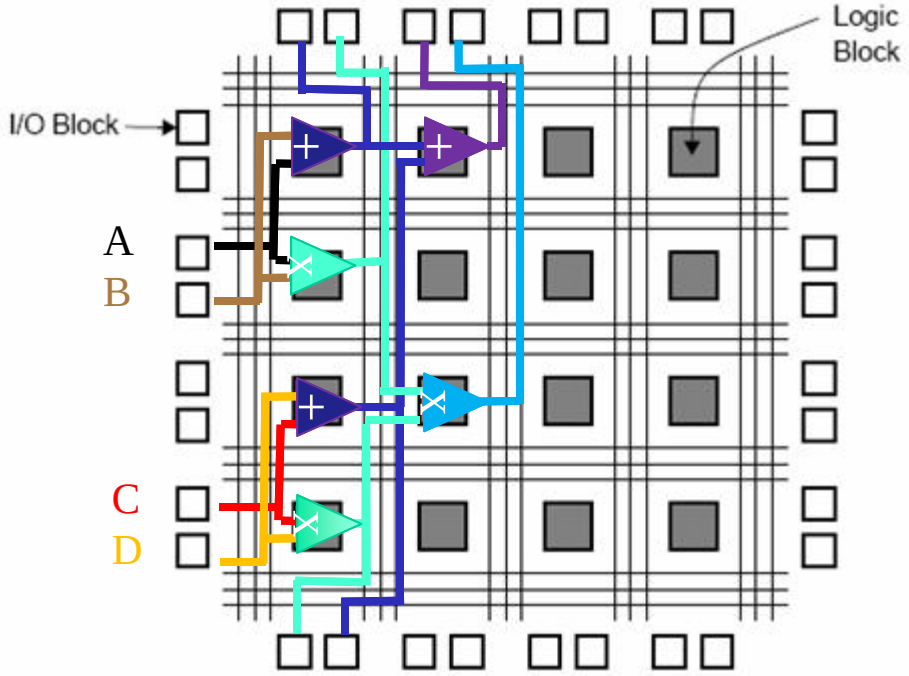
Each **Logic block** of an FPGA can be configured to provide functionality as simple as that of transistor (switch) or as complex as that of a microprocessor. Each block can implement different combinations of combinational and sequential logic functions.

In a very simple view, operation of the FPGA includes:

1. Preprogramming the array, creating a configuration file and downloading it to the device.
2. A datum/address is read in
3. The system clock is cycled
4. (changing the "state" of the machine)
5. Output may be available …
6. Return to Step 2



Complex Detector Electronics: FPGA's

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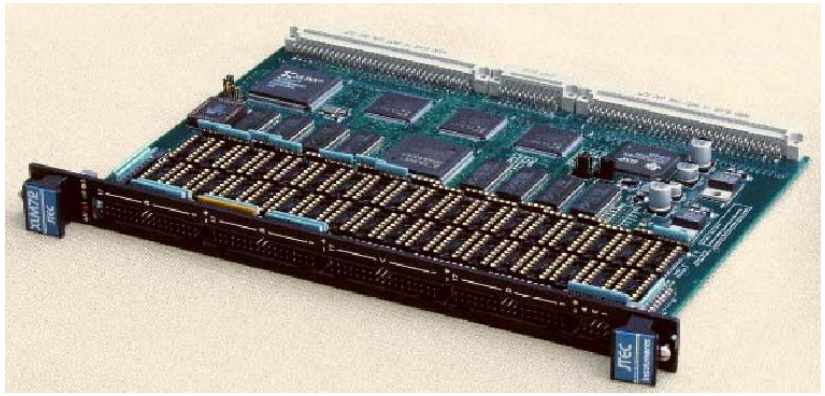
Field **P**rogrammable **G**ate **A**rrays can be found in CAMAC and VME packages … the programming is done externally (generally with a simulation code running on a PC) and the result has to be loaded over the backplane.

LeCroy 2366 is a CAMAC-based logic module with 59 ECL lines and a Xilinx 4005 FPGA chip. Any logic that can be implemented as a synchronous (clocked) state machine may be programmed, subject only to the limitations of the size of the Xilinx gate array chip (approximately 5000 gates, current devices have 100x more gates).



Jtec XLM72 is a universal logic VME module using a FPGA executing fast synchronous and combinatorial logic, a 900-MFlops/s floating-point Digital Signal Processor (DSP) executing complex numerical calculations, two 2-Mbyte banks of fast memory, and 72 ECL I/O ports.

Complex Electronics: “Digital Acquisition-1”

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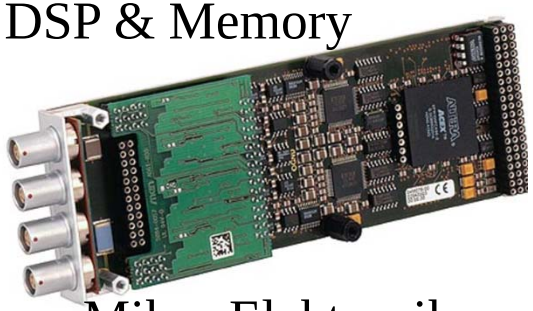
Tektronics Digital Scope

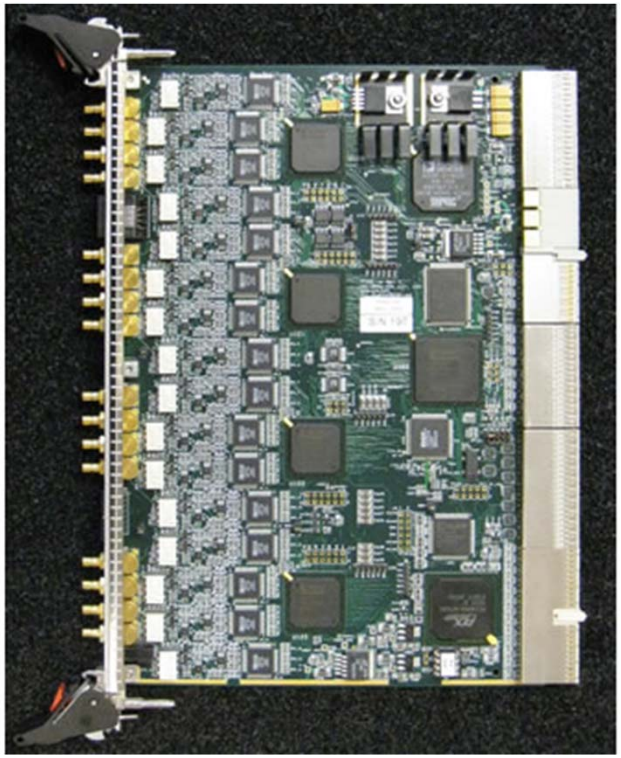
Agilent VME device: E1438C/D
100 MSa/s Digitizer, DSP & Memory



Agilent 1GSa/s

Mikro Elektronik
M78 4chan O-scope
50Msps,12bit

ChargerLab
voltage monitor



XIA Pixie-16 – dedicated nuclear physics orientated DAQ device – 16 channels are digitized in a 12-bit ADC at a rate of 100MHz (10 ns). Triggering, pile-up inspection and filtering of the data stream is performed in real time; pulse heights and other event data is calculated on an event-by event basis. Results are stored in 512K of spectrum memory and 128k of list mode FIFO memory.

Complex Electronics: "Digital Acquisition-2a"

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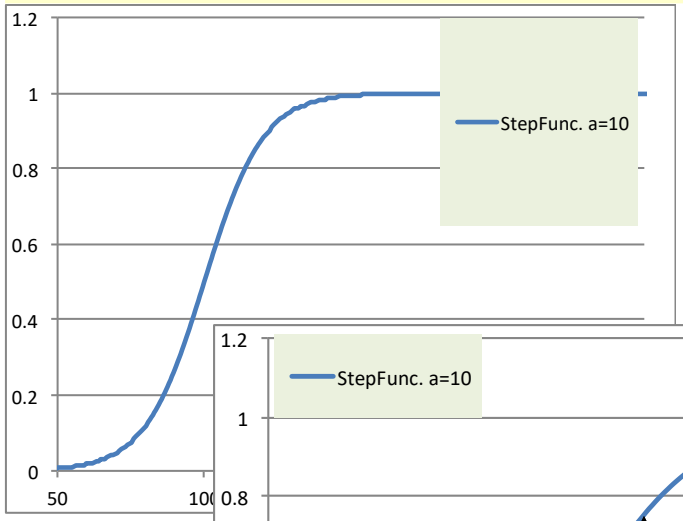
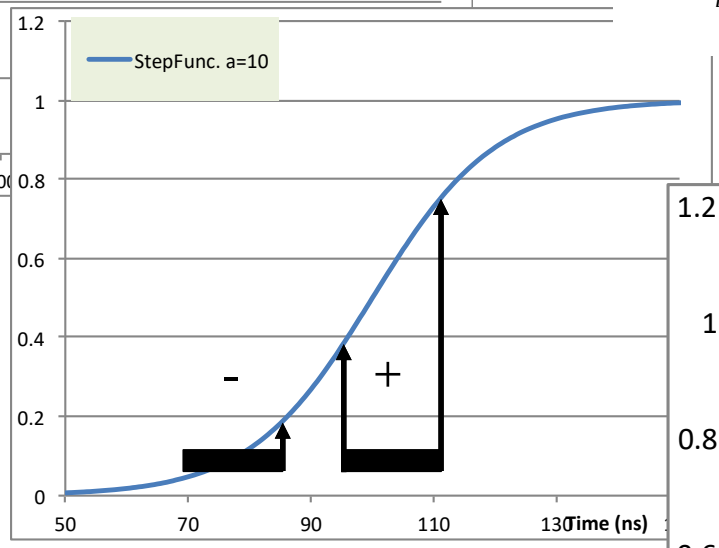
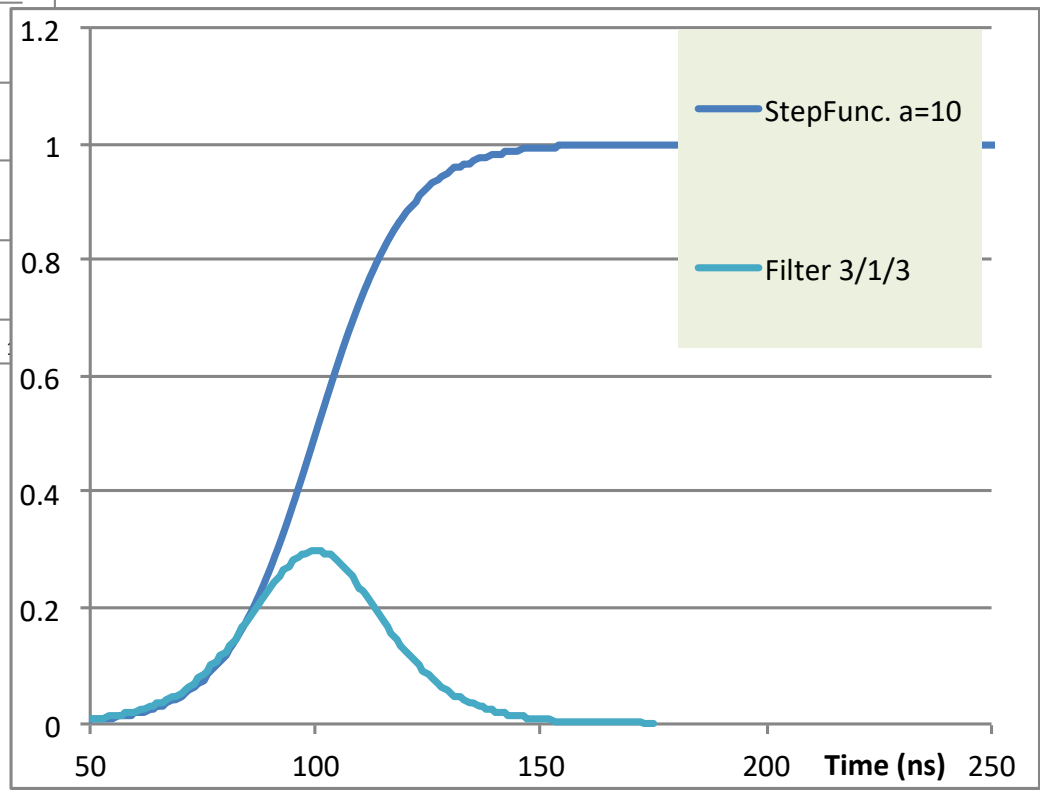




$$Trace_i = \left(\frac{Q}{C}\right)\frac{1}{1+e[-(t_i - t_0)/a]} \qquad t_0 = 100ns,\ a = 10ns$$

$$Filter_i = \sum_{j=i-(L-1)}^{i} Trace_j - \sum_{j=i-(2L+G-1)}^{i-(L+G)} Trace_j \qquad 'L'ength,'G'ap$$



all times in ns
Δt = 1ns (1GHz trace)

Complex Electronics: “Digital Acquisition-2b”

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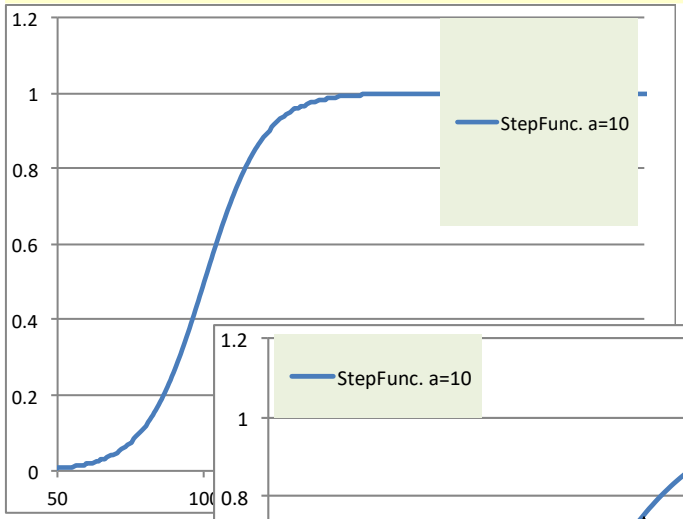

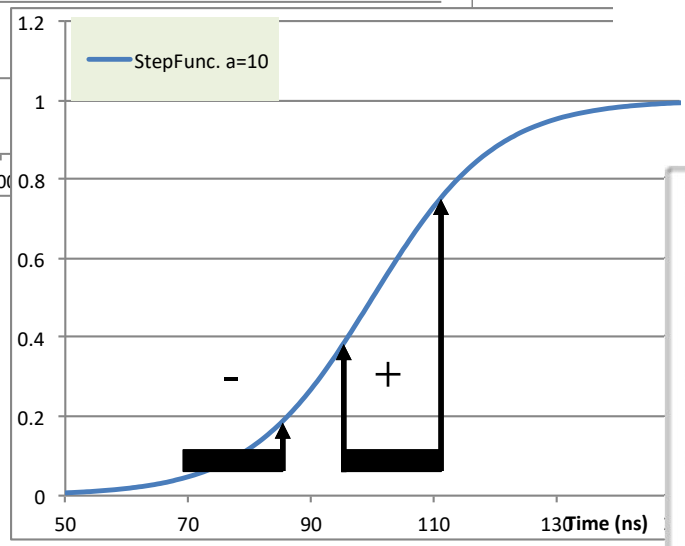

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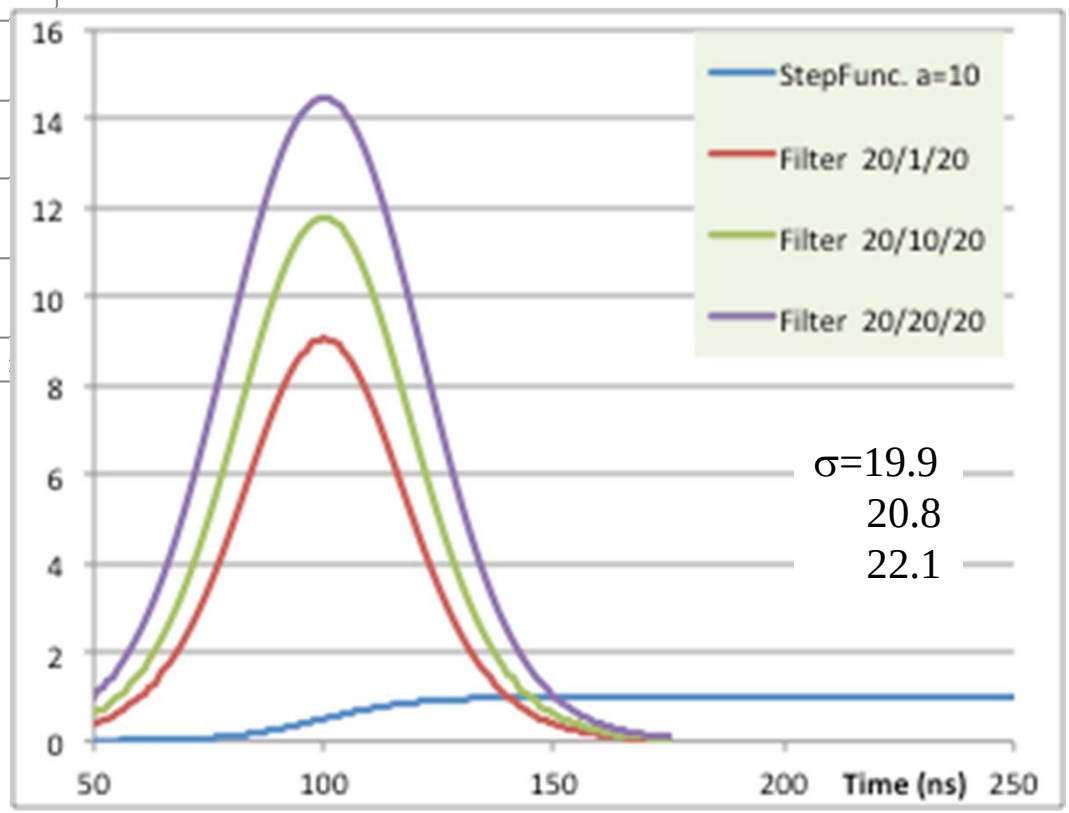
$$Filter_i = \sum_{j=i-(L-1)}^{i} Trace_j - \sum_{j=i-(2L+G-1)}^{i-(L+G)} Trace_j \qquad 'L'ength,'G'ap$$



all times in ns
Δt = 1ns (1GHz trace)

Change “Gap”

Complex Electronics: “Digital Acquisition-2c”

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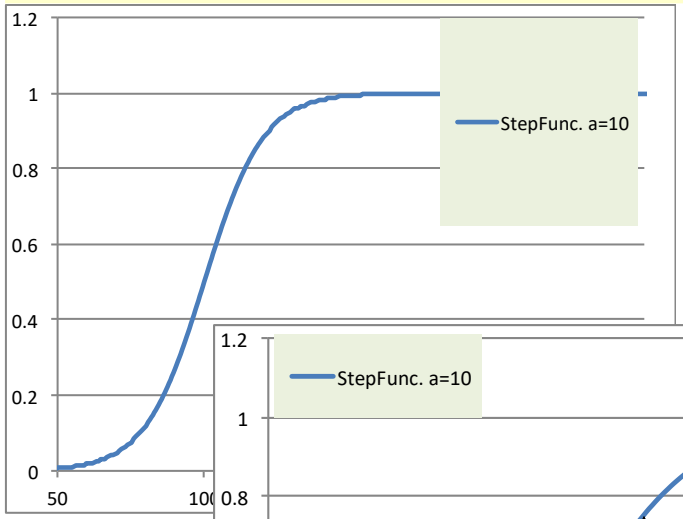

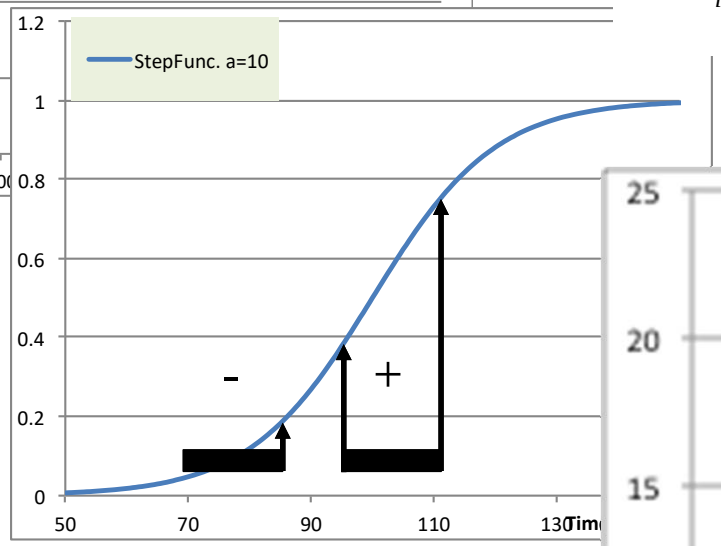

$$Trace_i = \left(\frac{Q}{C}\right)\frac{1}{1+e[-(t_i - t_0)/a]} \qquad t_0 = 100ns,\ a = 10ns$$

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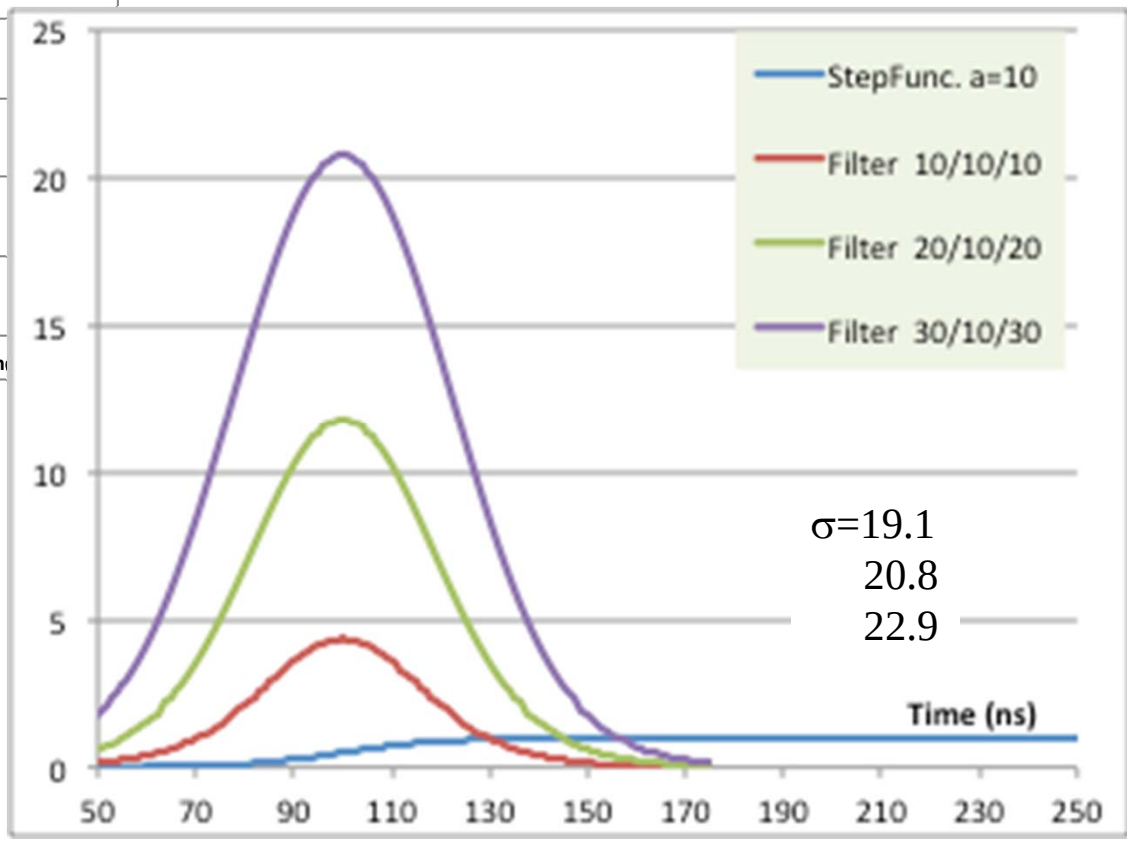
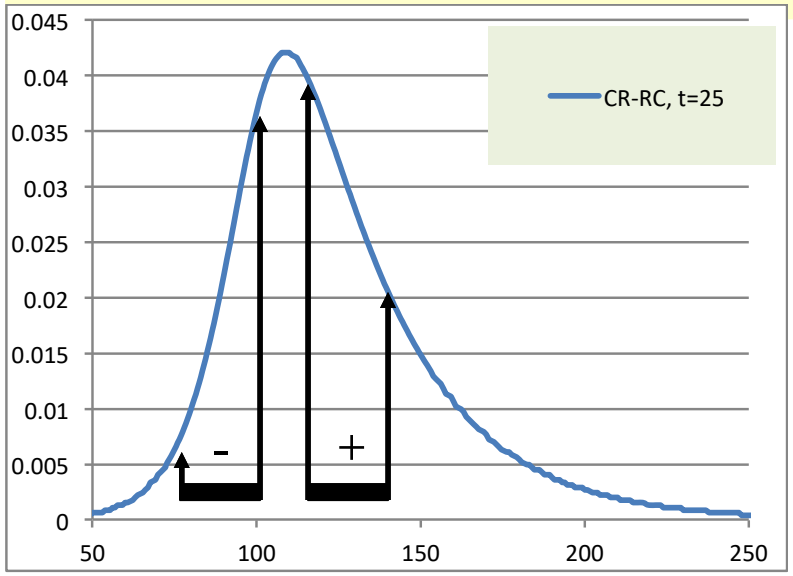


all times in ns
Δt = 1ns (1GHz trace)

Change “Length”

Complex Electronics: “Digital Acquisition-2d”



$$Trace_i = \left(\frac{Q}{C}\right)\frac{1}{1+e[-(t_i - t_0)/a]}\left(\frac{t_i}{\tau}\right)e^{-t_i/\tau}$$

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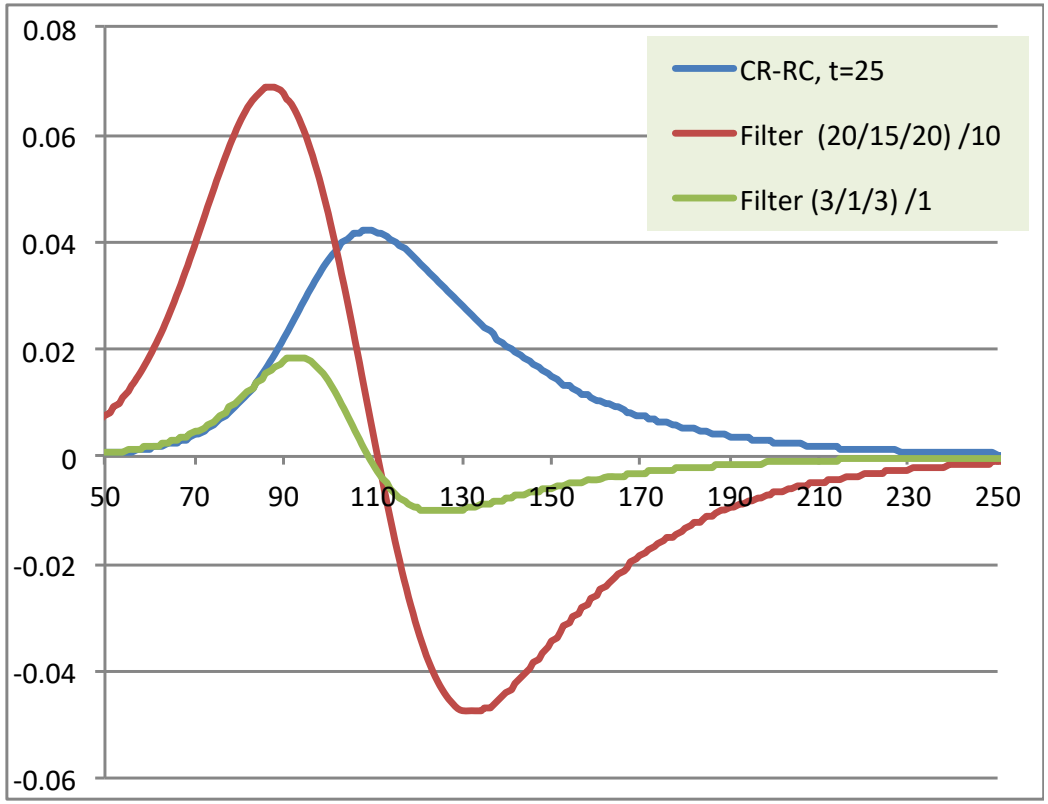
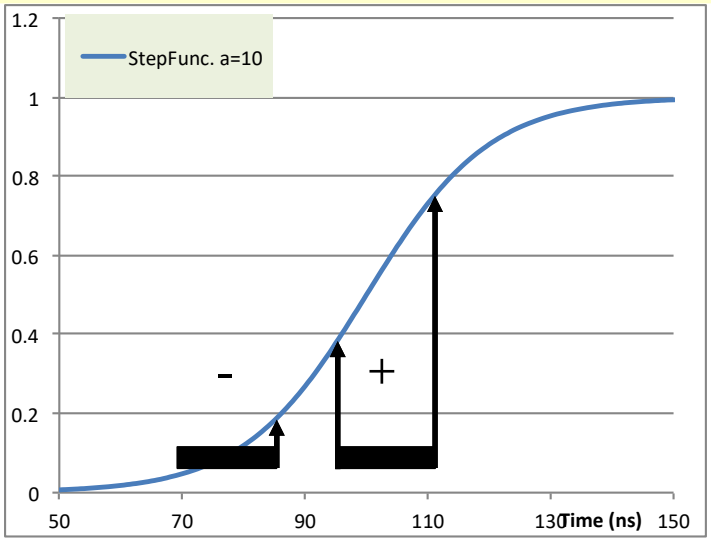


all times in ns
Δt = 1ns (1GHz trace)

Change Input pulse

Complex Electronics: “Digital Acquisition-2e”

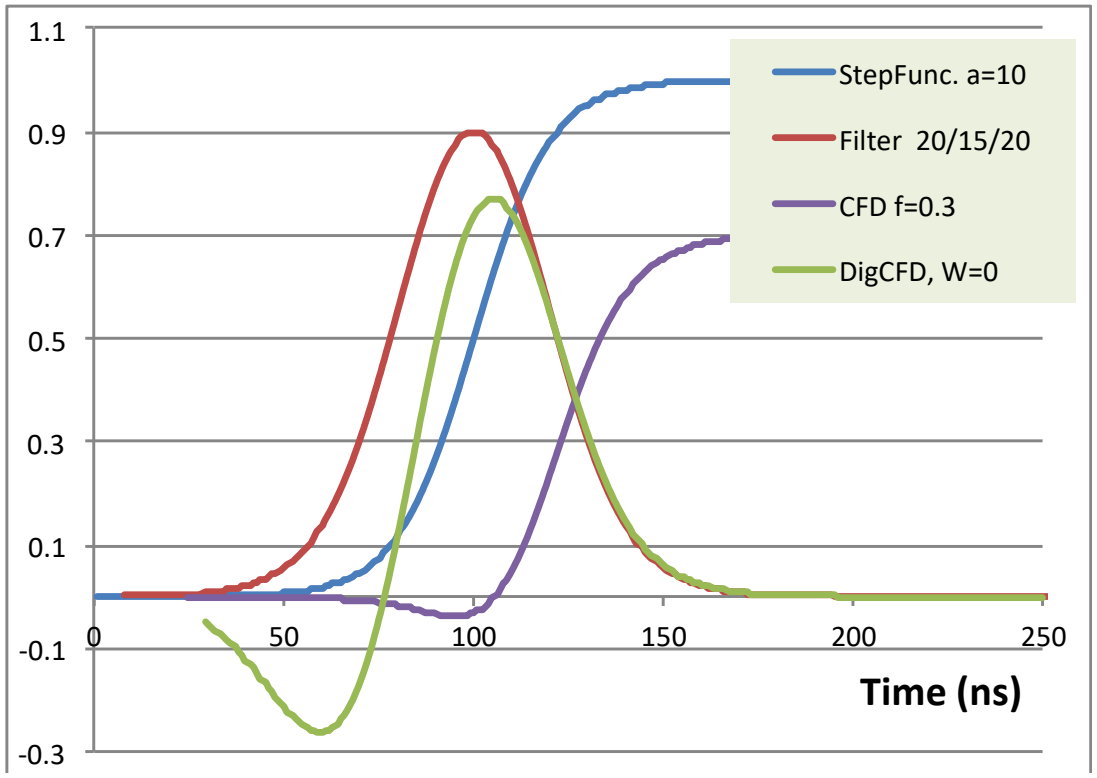


$$Trace_i = \left(\frac{Q}{C}\right)\frac{1}{1+e[-(t_i - t_0)/a]}$$

$$Filter_i = \sum_{j=i-L+1}^{i} Trace_j - \sum_{j=i-2L-G+1}^{i-(L+G)} Trace_j$$

$$"CFD_{i+D}" = F_i - \frac{F_{i-D}}{2^{W+1}} \qquad D \rightarrow Delay, W \rightarrow Weight$$

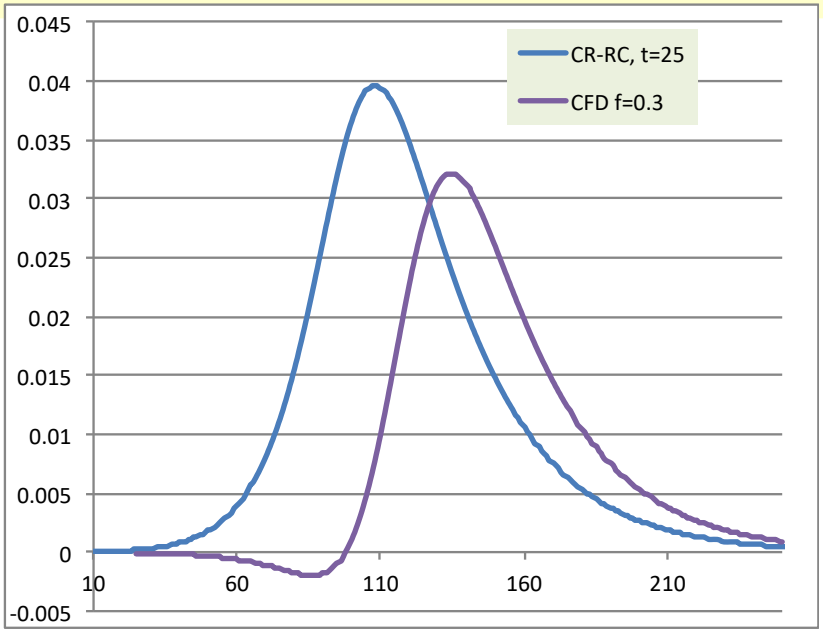
$$CFD_i = f\,Trace_i - Trace_{i+Delay} \qquad f \rightarrow fraction$$



all times in ns
Δt = 1ns (1GHz trace)

Create “CFD” output

Complex Electronics: "Digital Acquisition-2d"



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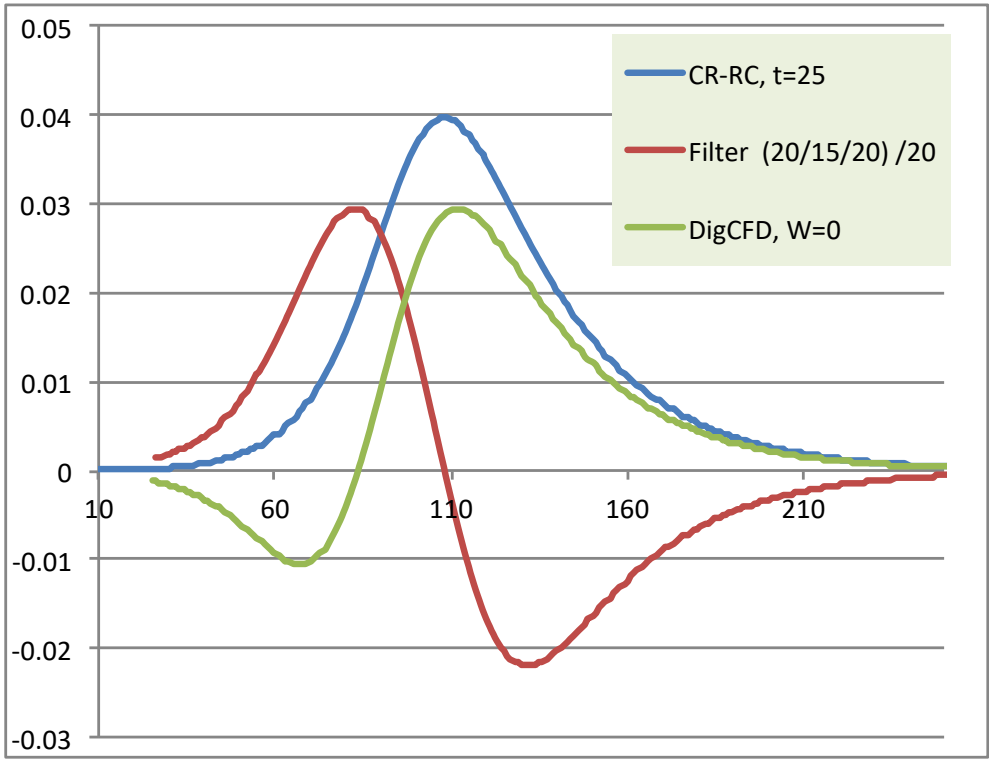
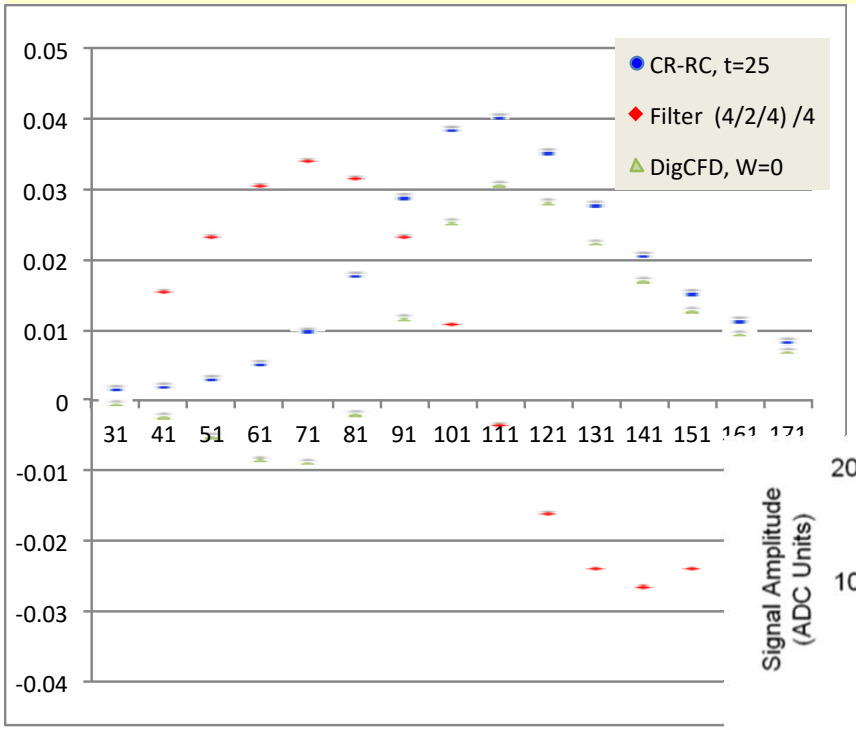


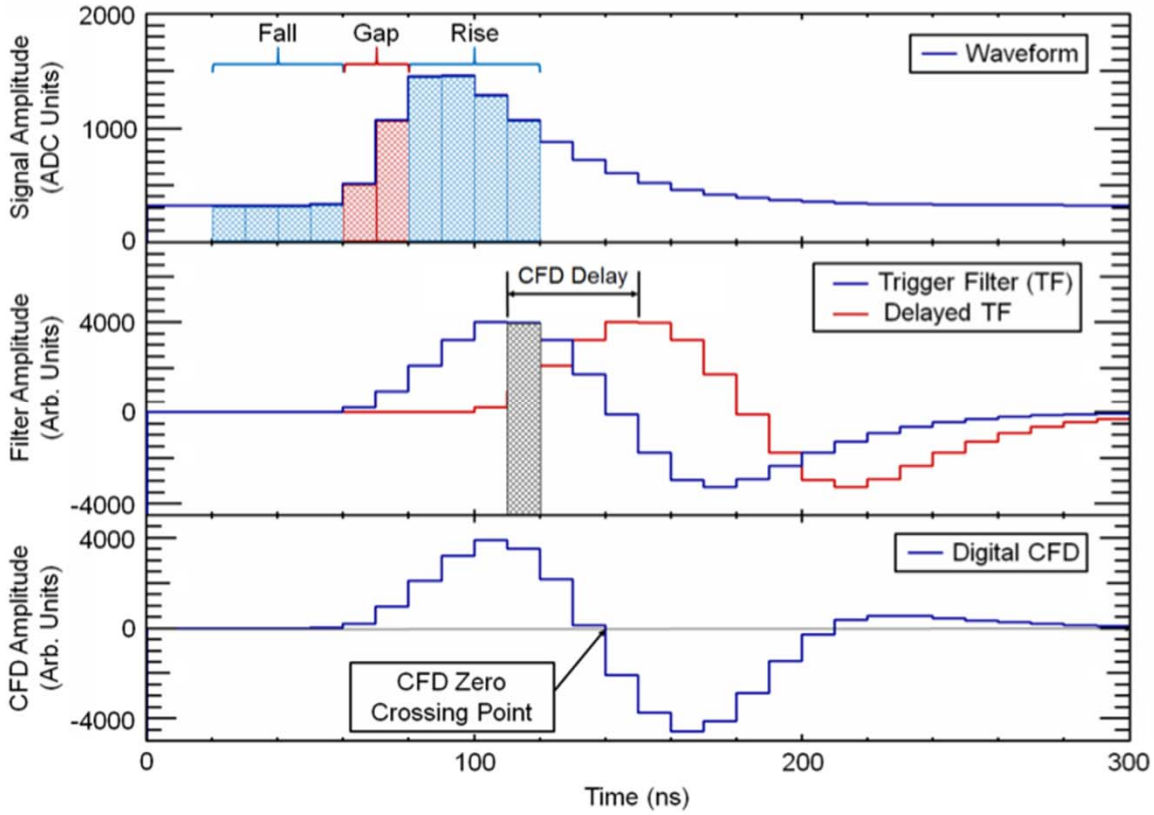
all times in ns
Δt = 1ns (1GHz trace)

Complex Electronics: “Digital Acquisition-2e”



Yesterday, with 100 MHz traces available
… today 250, 500 MHz traces …
(Previous traces sampled every 1ns, 1GHz)

Real example from Chris Prokop, DNP-2013



all times in ns
Δt = 10ns (100MHz trace)

Complex Detector Electronics: HiRA Example

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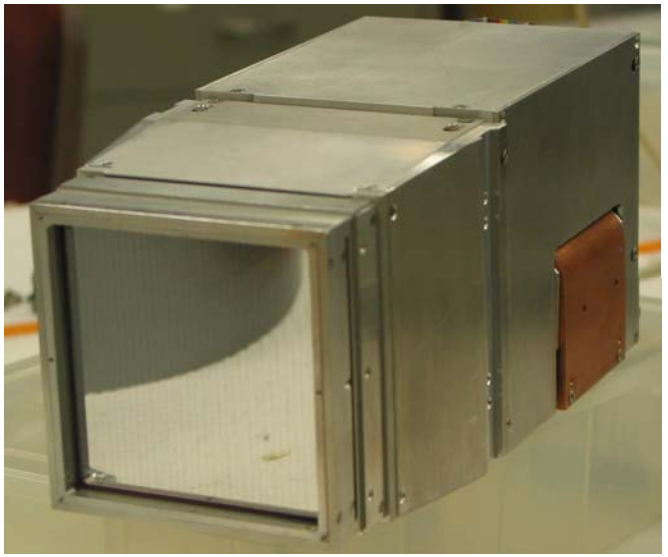

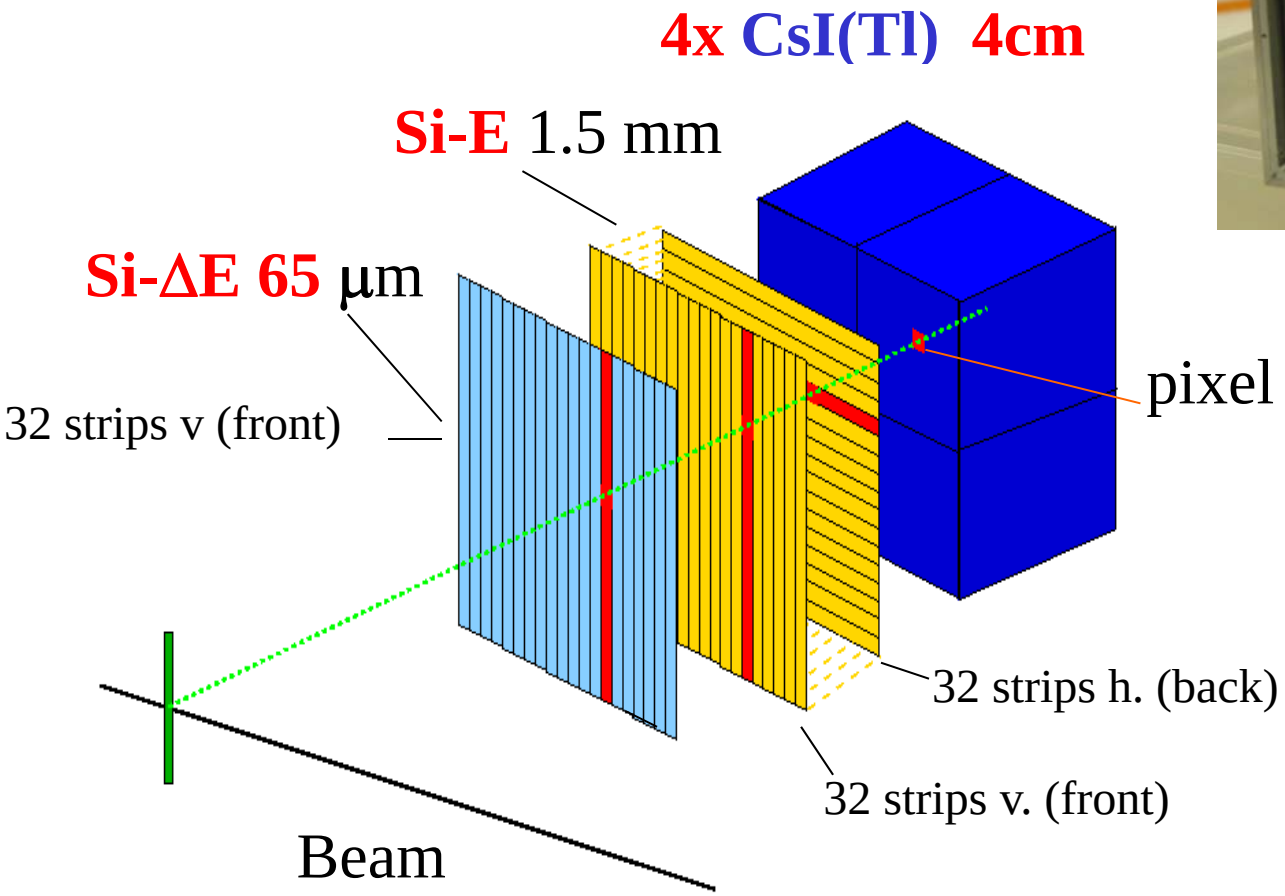

- **20 Telescopes**
- **62.3 x 62.3 mm^2 Active Area**
- **strip pitch 1.8 mm**
- **1024 Pixels per telescope**

Complex Detector Electronics: HiRA ASIC

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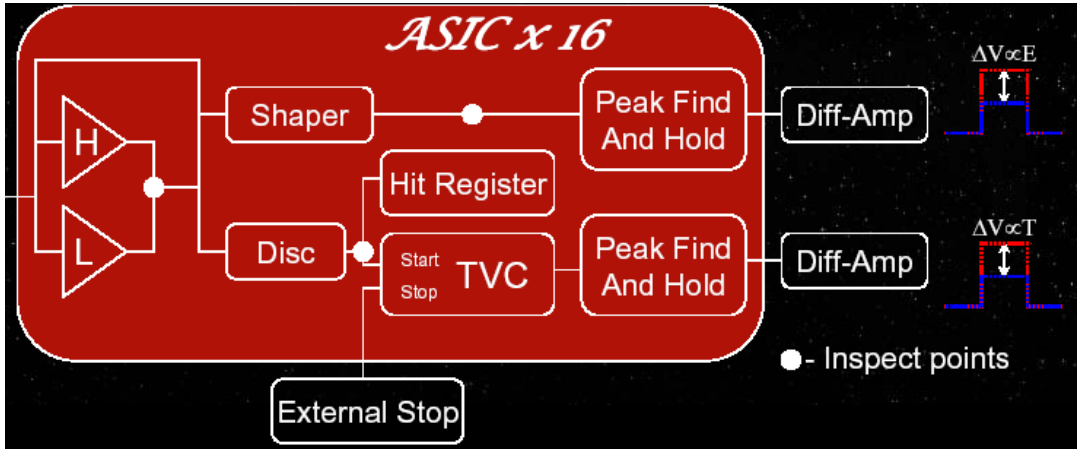
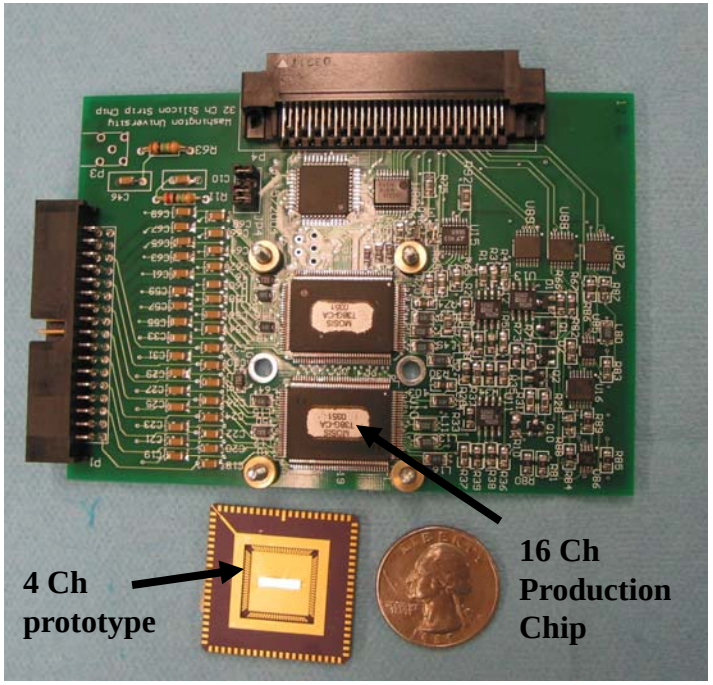
Developed at Washington University (St. Louis) and Southern Illinois University, this chip board (differential signal output) + one VME module (SIS 14-bit flash ADC) replaces 64 pre-amp's, 32 Shapers, 32 TDCs and 32 ADCs

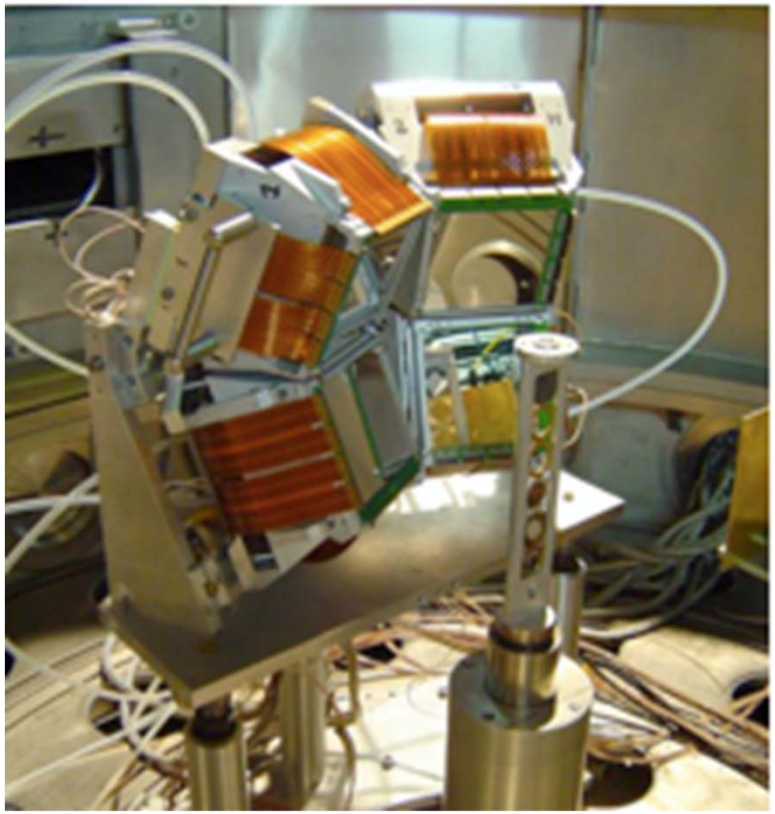


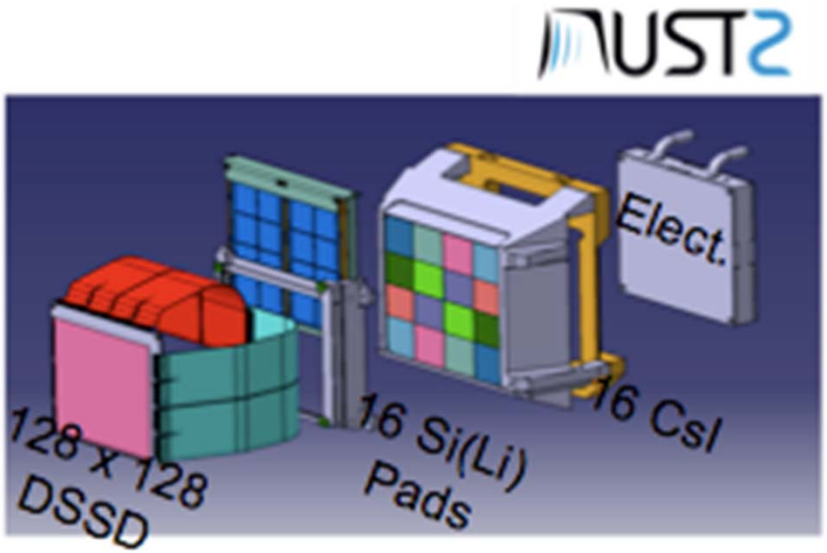


- Input is switchable, charge-sensitive [x1, 100 MeV(Si), x500MeV(Si)]
- Shaper x1 with 1μs shaping time
- Time-to-voltage signal against "stop" signal [150 ns, 1.5μs FS]
- Both outputs are held for external sampling by flash ADC

Test by M.Wallace showed 50 keV resolution for ^{228}Th source …

Complex Detector Electronics: MUST2





- 100 cm^2 area on front face
- 288 channels of Energy and Time (each)
- Si 300 μm / Si(Li) 5mm / CsI 4cm

Project **MUST2** (**MU**r à **ST**rips) is a multidetector of 10 telescopes; each telescope is made up with two X and Y plans of 128 Si tracks followed by 16 SiLi and 16 CsI. MUST2 is dedicated to the study of the light products produced from the interaction of radioactive beams with a target.

Complex Detector Electronics: MUST2

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Asic solution for the Si, Si(Li) and CsI signals

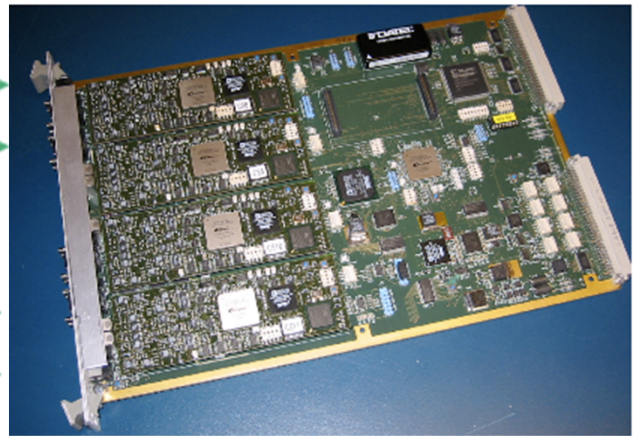
MATE

- 16 ch (E & T)
  - Bipolar
  - Energy
    - Shaping: 1µs/ 3µs
    - Range: 10 - 200 MeV
    - 20 keV FWHM (gene)
  - Time
    - Leading Edge
    - TAC (300 / 600 ns)
    - 300 ps FWHM (gene)
- Slow Control (I2C)
- Inspection (Debug)
- Chip 36mm²
  - BCMOS 0.8 µ
  - 16000 transistors
  - 35 mW/ch
- Serial output 2 MHz

MUFEE
(2x per tel)

9x MATE
1x bus I2C
2x analog bus (Idif)
1x control line
Internal generator
Temperature probe

MUVI
(4x tel)

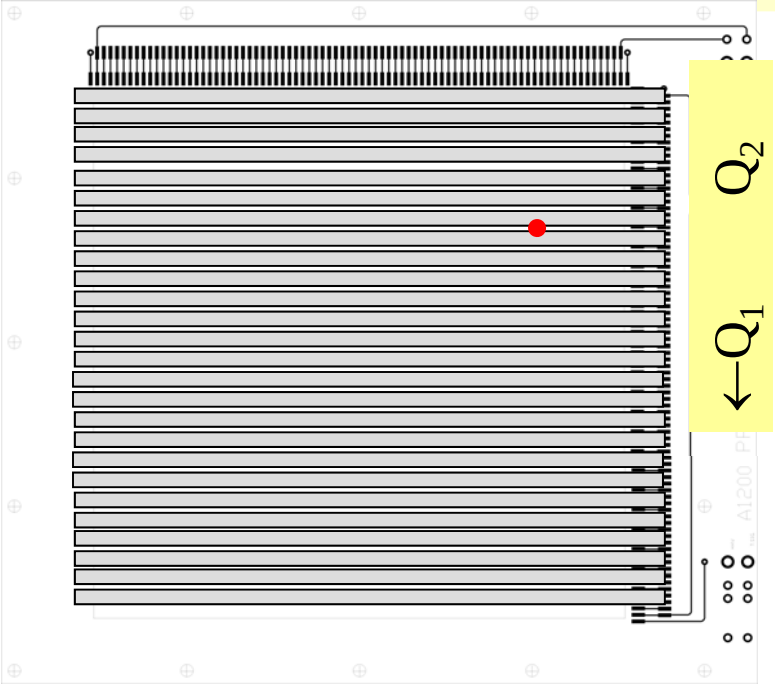


4x CAS
576 parameters
4 ADC 14 bits, **100µs DT**
Slow Control, C&C (DAC)
Scalers, Inspection
Time stamping (ATOM)

MUST2 Electronics is based on ASICs (Application Specific Integrated Circuit) so called **MATE**. MATEs are housed on **MUFEE** cards located closed to the detectors. In each MATE 16 detector channels are analog processed in order to get the 16 energy (E) and 16 time (T) analog steps . These steps are serially sent to MUVI.

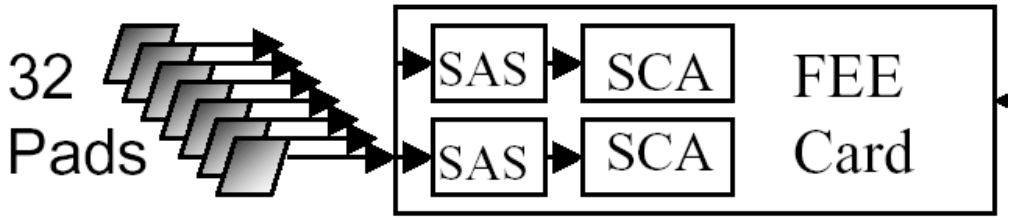
MUVI is a C sized VXI card in which are implemented the 14 bits analog to digital conversion, the digital processing, the physics parameters readout and the MATEs control. MUVI was specially designed in order to pay attention at the aspects of resolution, density of channel and reduction of the dead time of acquisition. It manages 4 telescopes and delivers more than 2000 E and T parameters processed in 4 **CAS** daughter cards.

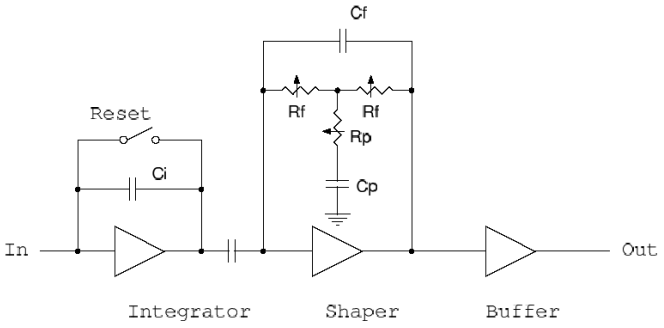
Complex Detector Electronics: PPAC's ?



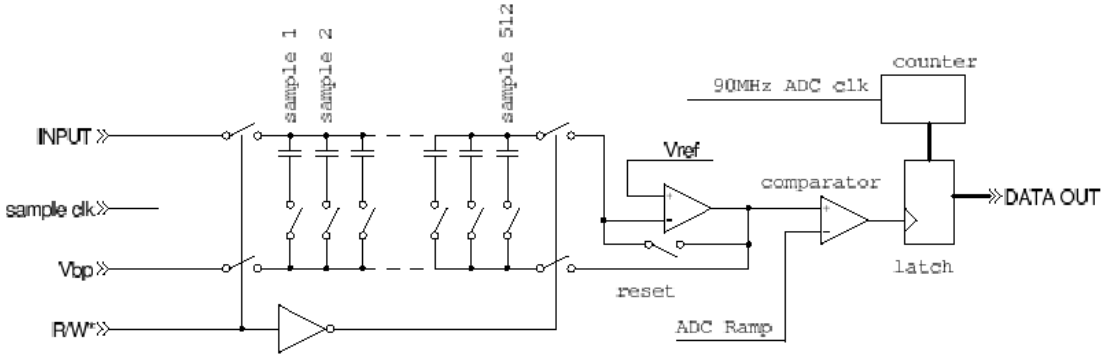
Conventional: resistor chain, two linear channels
Problems with small signals, large size – many resistors

STAR Front-End Electronics (134k channels)
http://arxiv.org/abs/nucl-ex/0205014
And
http://www.star.bnl.gov/public/fee/fee.html



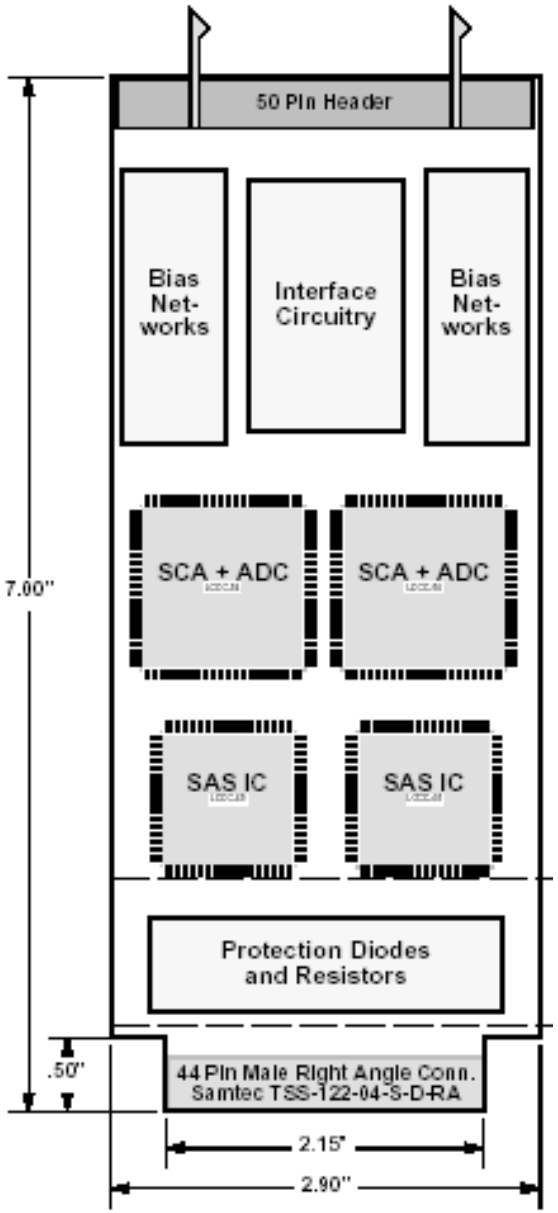


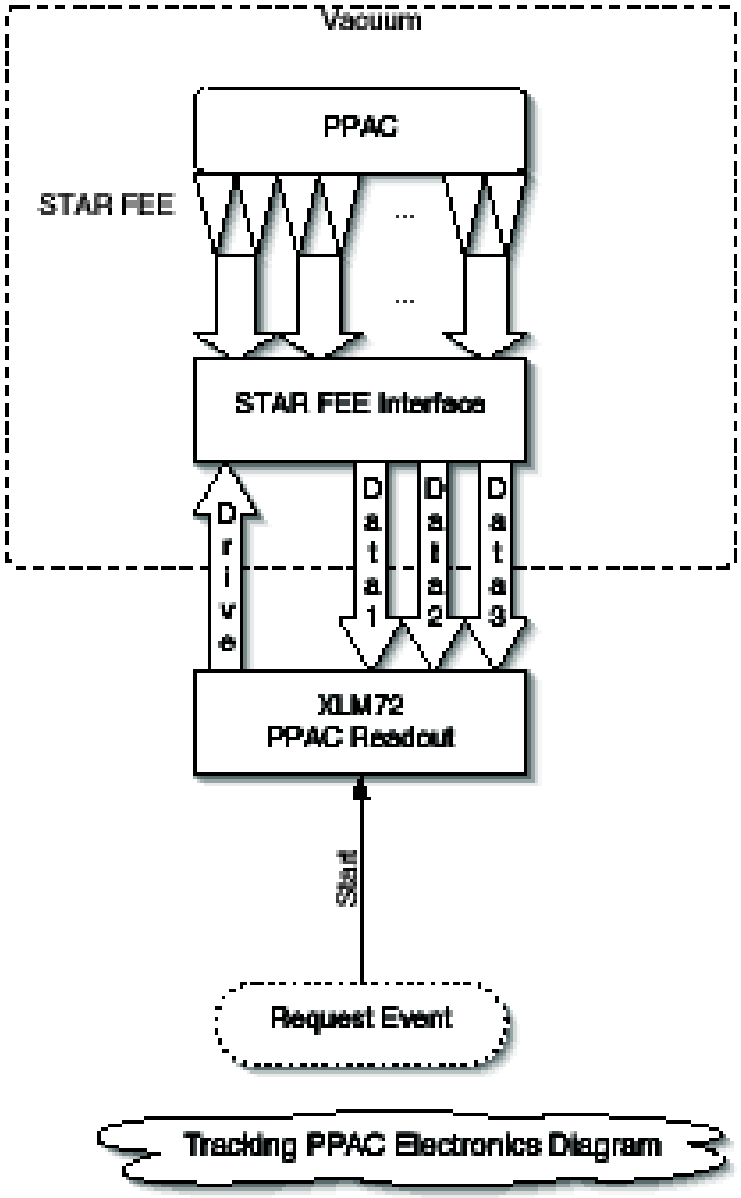
Preamp/Shaper (SAS)



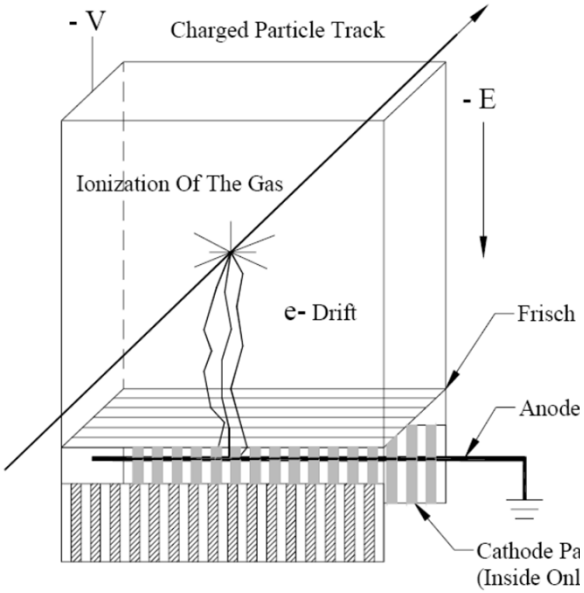
Switched Capacitor Array & ADC (SCA)

Complex Detector Electronics: ASIC's



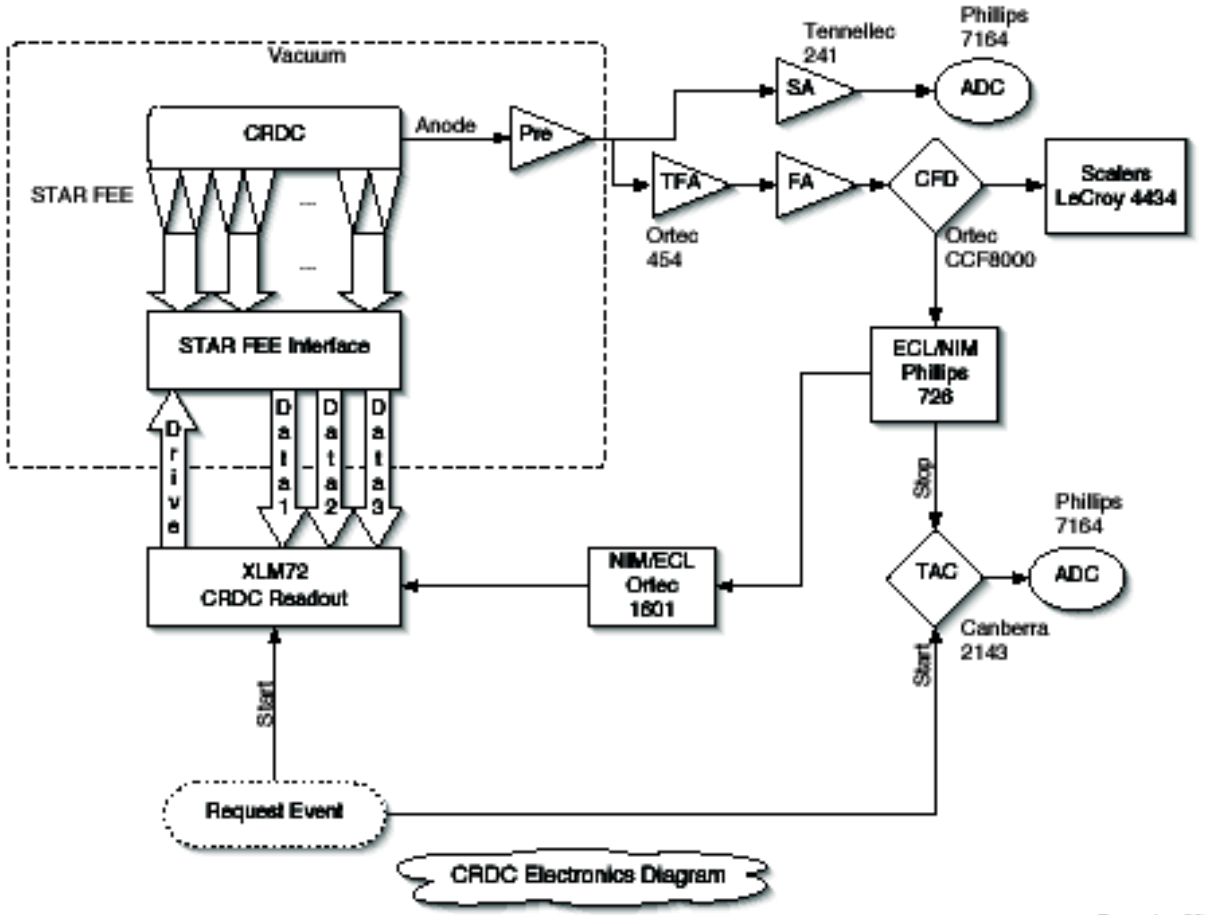


Complex Detector Electronics: CRDC Pads



(C.Freigang, MSU thesis, 2oo1)

Schematic diagram of Cathode-Readout Drift-Chamber used in Sweeper & S800 focal plane detectors



Chap. 18c – Data Acquisition: Question

Given the following schematic diagram, what conversion type (algorithm) is used in the STAR-FEE card? What is the average conversion time of the (12-bit, 2mV V_{LSB}) ADC that is part of the STAR-FEE card?