Analysis, A to D

Multidimensional DAQ
-- Trigger logic
-- A1900 minimum PID
-- Data stream
-- Electronics standards
-- Real-time computing
-- Architectures

High Dimensional Detector Electronics

https://midas.triumf.ca/Midas Wiki/index.php/Main_Page

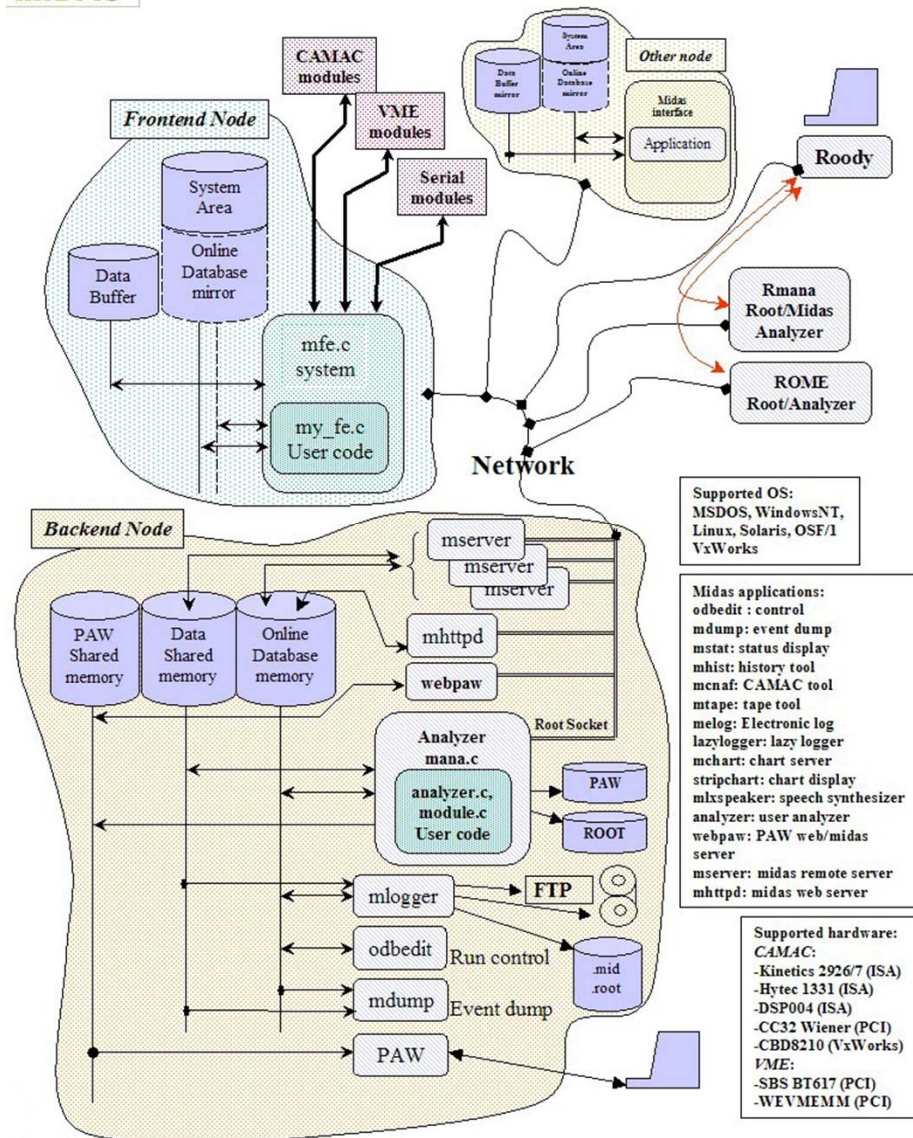MIDAS : Maximum Integrated Data Acquisition System
http://midas.psi.ch   Stefan Ritt   midas@psi.ch
http://midas.triumf.ca   Pierre-André Amaudruz   midas@triumf.ca

Chap. 18b – Data acquisition

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The first question to ask is "do I have more than one detector?" ..

No – simple situation, use a multichannel analyzer (MCA) described in text. In a gross overview this device is an ADC connected to a digital memory that keeps track of the number of signals that fall into each bin (V_{LSB} steps) of the ADC. Most of the hardware is associated with the display of the data in memory. (Modern devices are contained on a PCI card or more commonly a stand-alone with a USB connection.)
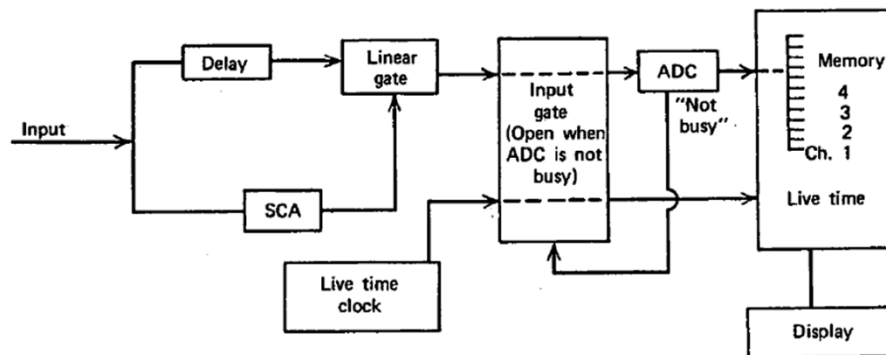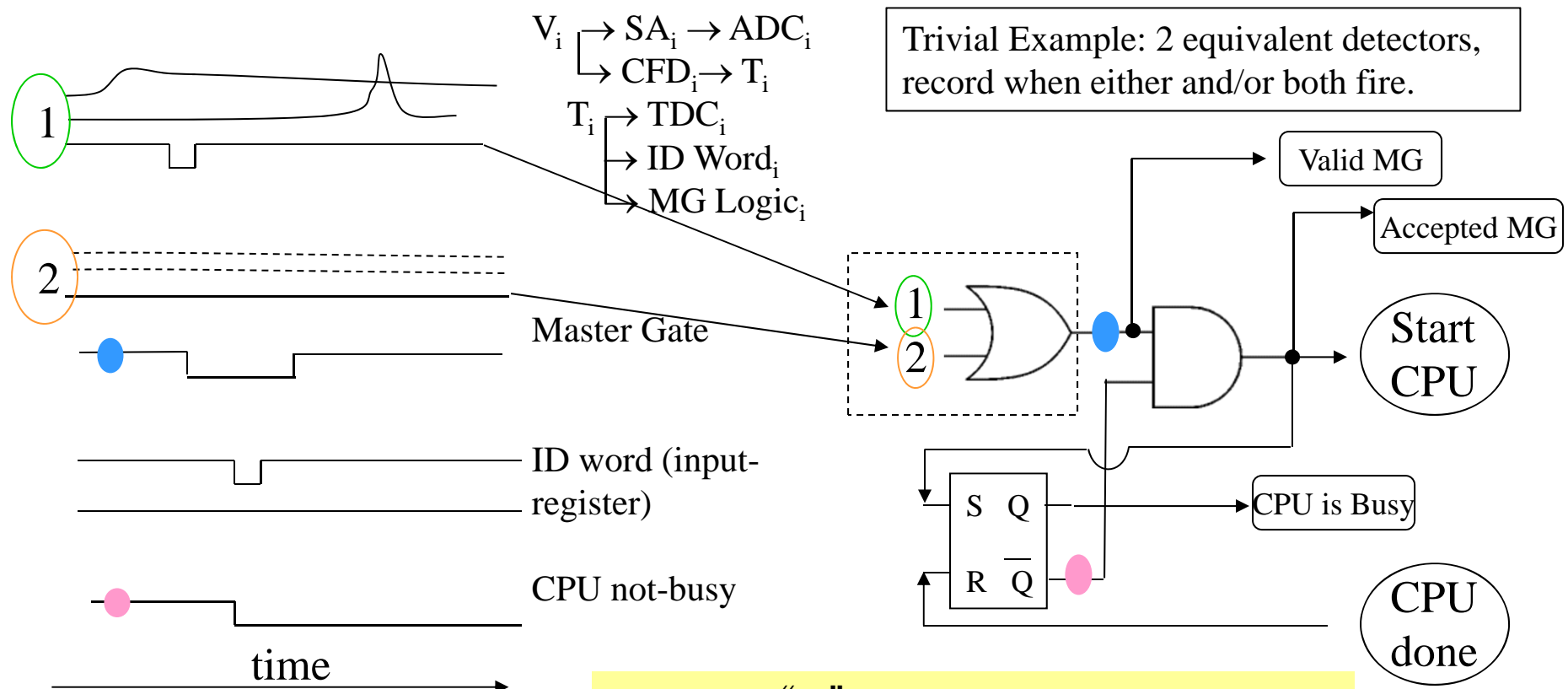

Fig. 18.7 Knoll, 3rd, 4th Eds.

Yes – more typical situation in nuclear science, generally want to retain correlations among the input signals. Up to present electronics/data recording are not fast enough to record literally everything (but getting close). The experimenter has to set up some electronic logic to decide when to process and/or record the data. This is called "Real Time" computing.
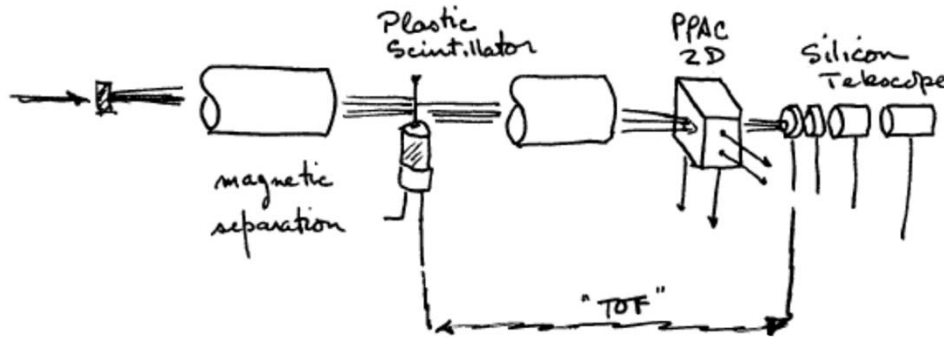
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The "trigger logic" is programmed to decide when to process and record the data.
- The output of this logic system is usually called the "master gate."
- The logic usually also provides "guidance" to the CPU about processing the event.
- The logic needs to provide a way to monitor the number of lost signals.
- The logic itself can range from individual modules to a digital logic device.
- Important logic units are AND, OR (Fan-in), LATCH, Gate & Delay Generator

$V_i \rightarrow SA_i \rightarrow ADC_i$
$\hookrightarrow CFD_i \rightarrow T_i$
$T_i \rightarrow TDC_i$
$\rightarrow$ ID Word$_i$
$\hookrightarrow$ MG Logic$_i$

Trivial Example: 2 equivalent detectors, record when either and/or both fire.

Valid MG

Accepted MG

Master Gate

Start CPU

ID word (input-register)

CPU is Busy

CPU not-busy

S   Q
R   Q̄

CPU done

time

User has to "or" all contributions to total deadtime

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Data Acquisition: PID in A1900

Particle ID depends on measuring:

ToF $\rightarrow$ v or β and γ

$B\rho \rightarrow m\,\beta\,/q$ $\qquad ^{m}Z^{q}$

$\Delta E \rightarrow mZ^{2}\,/\,E$ $\qquad$ (Z,q integer)

E-total $\rightarrow$ ½ $m\beta^{2}$
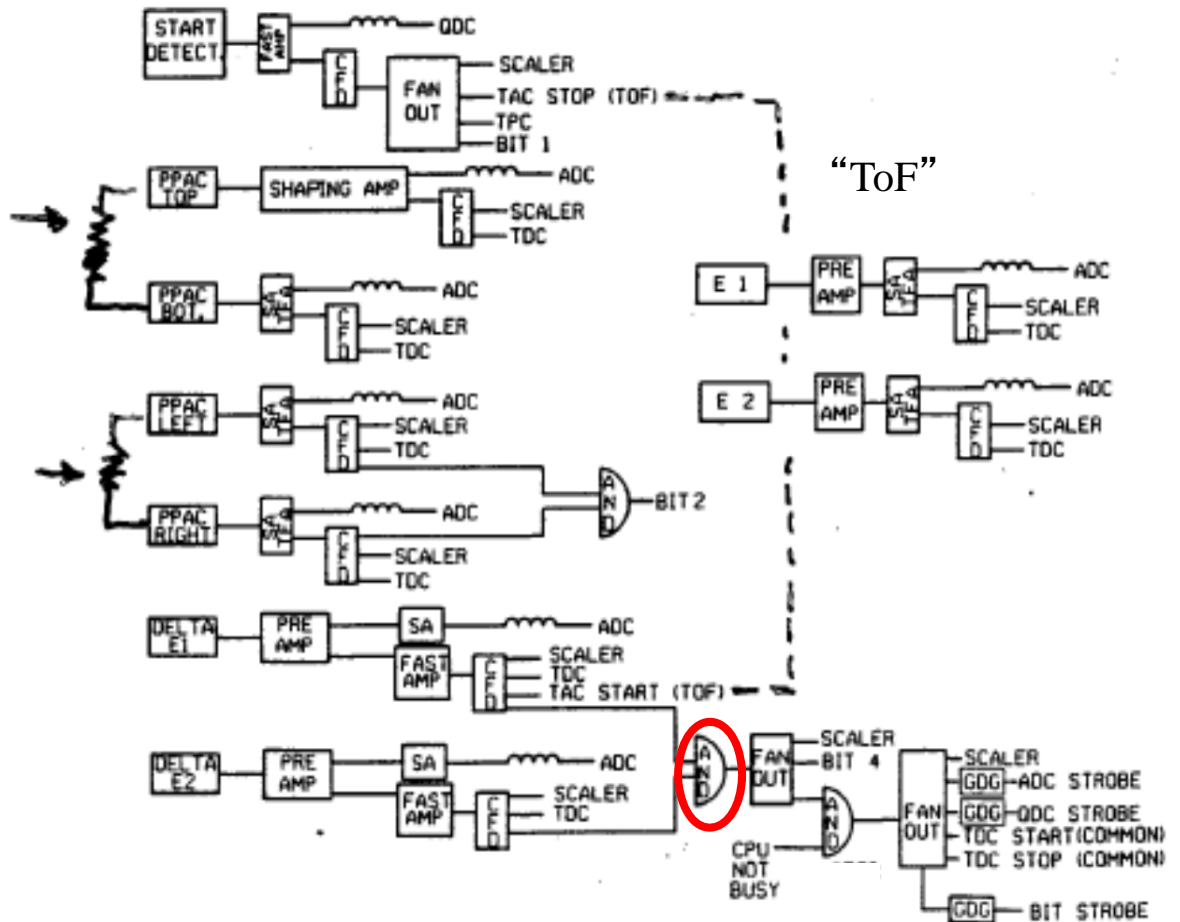
Notes:

PPAC's use charge-division

Bit Register (input reg., pattern reg.)
TAC for precise ToF (stop/start)
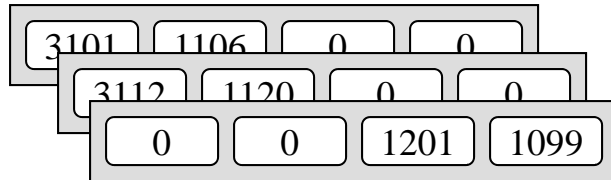(time runs "backwards")

MG is one "AND"
Scalers keep count without gates

Data Acquisition: data stream

Options for Multidimensional data, simple example two detectors with E & T

1) Record all values in order including zeros as placeholders (n-tuple)

3101	1106	0	0
3112	1120	0	0
0	0	1201	1099

Example of 2 detector data stream, "energy" and "time"
Simple to interpret
"sparse" data (recall DSSD had 80 channels, only 2 valid)
error recovery from dropped words may be difficult

2) Record only non-zero words

A) embed information in data stream (plus word count, pattern register)

6	3	3099	1111	1221	1100
4	1	3101	1106
4	1	3112	1120
4	2	1201	1099
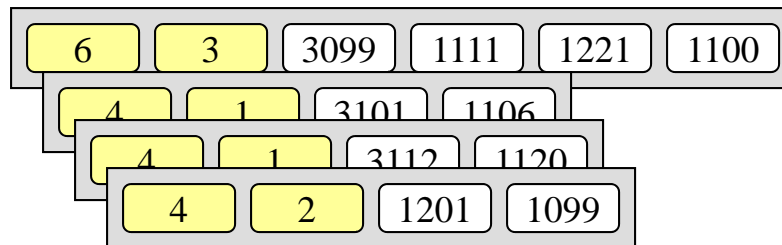
No gain for small experiments
Data needs to be "interpreted"
"dense" data

Problems from dropped words
are localized

B) embed information in data words (plus word count)

| 61443 | 38065 | 42059 |
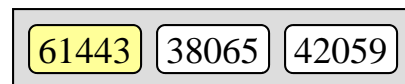
e.g. 16 bit word 4 bit ID, 12 bit data

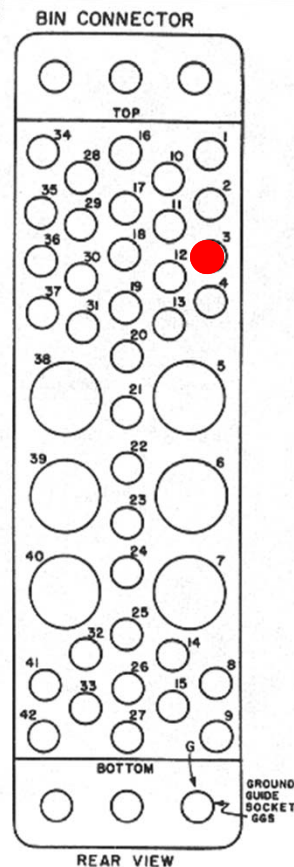| Binary | 1111 | 000000000011 | 1001 | 010010110001 | 1010 | 010001001011 |
| Hexidecimal | F | 003 | 9 | 4B1 | A | 44B |
| Decimal | 15 | 3 | 9 | 1201 | 10 | 1099 |

Data needs more "interpretation"
High level of error checking possible

Data Acquisition: Standards - NIM
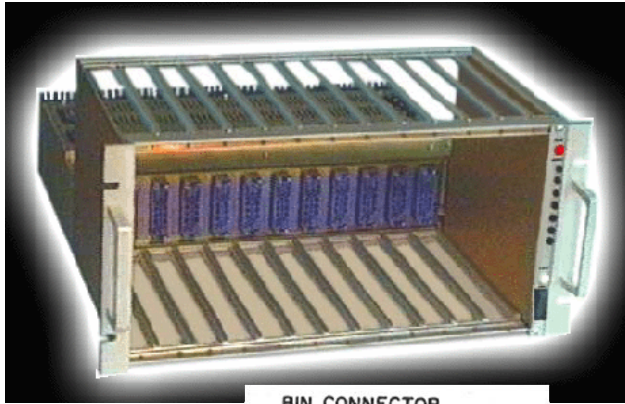
NIM (nuclear instrumentation module):
Nuclear Physics standard container/voltages/power
Only signal lines are Gate & Clear (not geographic)
Generally just a power supply. (All pins on the connector block are defined but not all are used or even wired. No data "bus.")

BIN CONNECTOR

TOP

REAR VIEW

GROUND
GUIDE
SOCKET
GGS

BOTTOM

Phillips Scientific

Constant Fraction Timing Discriminator

NIM MODEL 715

FEATURES
* Unexcelled Timing Characteristics
* Five Totally Independent Channels
* 100 MHz Operation
* Both Fast Veto and Bin Gate Inhibiting

MODEL 715 P\S
FIVE CHANNEL TIMING DISCRIMINATOR
MON. THRESHOLD IN

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U N I V E R S I T Y

NIM (nuclear instrumentation module):
Nuclear Physics standard container/voltages/power
Only signal lines are gate & clear (not geographic)
Generally just a power supply. (All pins on the
connector block are defined but not all are used or
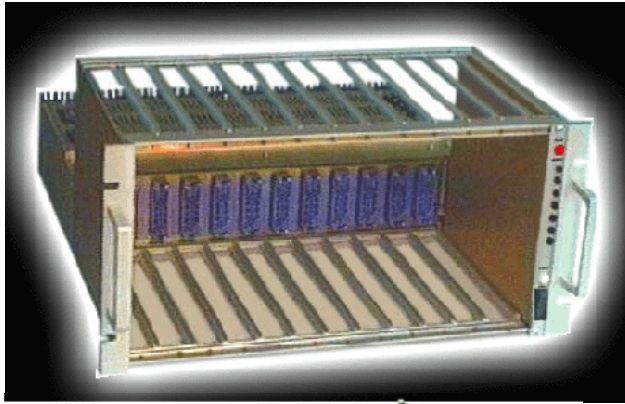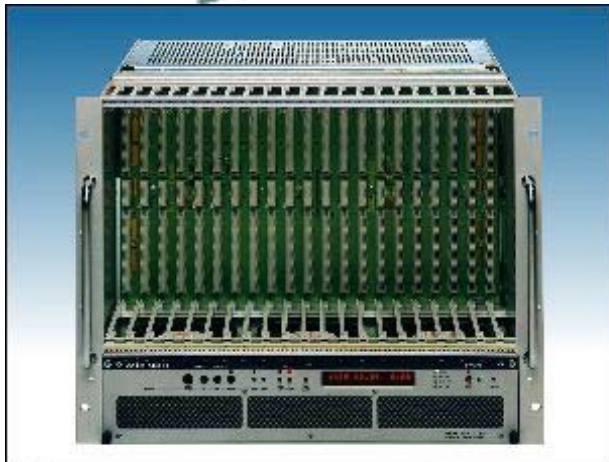even wired. No data "bus.")

CAMAC (computer automated measurement and control):
Nuclear Physics standard container/voltages/power
Computer bus (back plane) with [all 86 lines connected]
Address lines / write / read (24b) / control lines
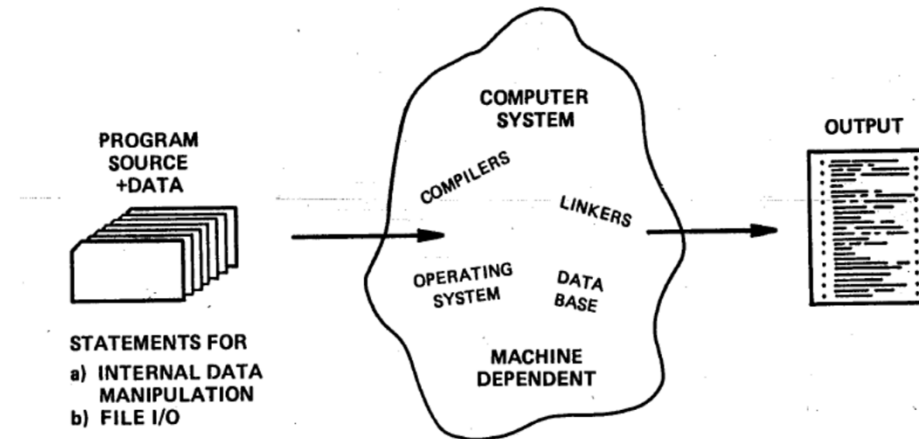Bus speed 1 MHz .. Geographic: "BCNAF" "LAM"

VME (Versa Module Eurocard):
industry standard container/voltages/power
Computer bus
Address lines (32b) / data lines (32b) / control lines
Bus speed 20 MHz ..
Not geographic (unless JAUX bus is used),
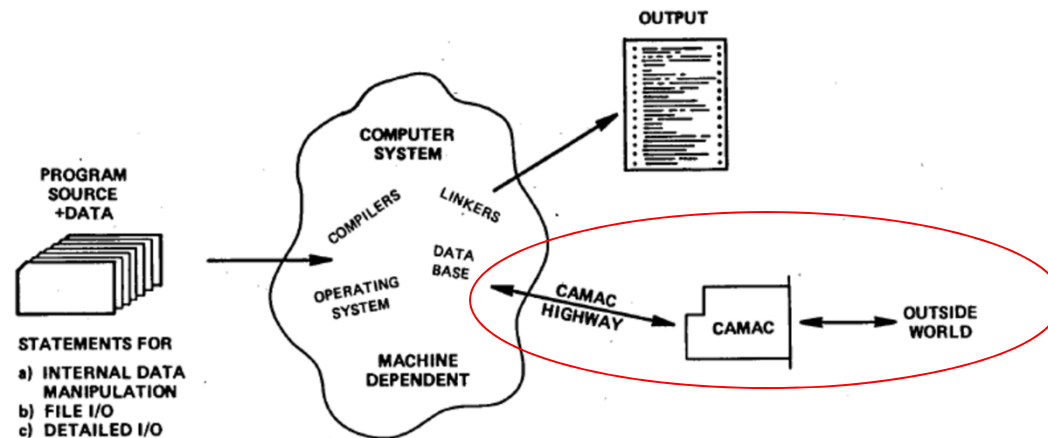Memory mapped … extensions VME64, VXI

Data Acquisition: Real Time Computing

From LA-UR-82-2718 "CAMAC Primer"

Conventional Program runs (once) in a constrained world .. even apparently interactive code such as spreadsheets have fixed input and are run once per "return character"

PROGRAM SOURCE +DATA

COMPUTER SYSTEM

COMPILERS

LINKERS

OPERATING SYSTEM

DATA BASE

MACHINE DEPENDENT

OUTPUT

STATEMENTS FOR
a) INTERNAL DATA MANIPULATION
b) FILE I/O

Real-time Program has to respond to environment and is fundamentally different. The codes spend a large fraction of time sampling input from "real world".

OUTPUT

PROGRAM SOURCE +DATA

COMPUTER SYSTEM

COMPILERS

LINKERS

DATA BASE

OPERATING SYSTEM

MACHINE DEPENDENT

CAMAC HIGHWAY

CAMAC

OUTSIDE WORLD

STATEMENTS FOR
a) INTERNAL DATA MANIPULATION
b) FILE I/O
c) DETAILED I/O

Data Acquisition: architectures – 1 –
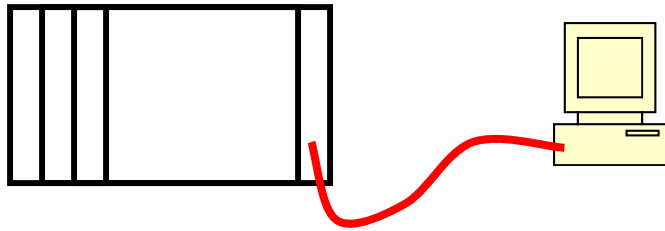
- GPIB (general purpose interface bus):
  IEEE-488 standard, 8-bit serial bus (slow)
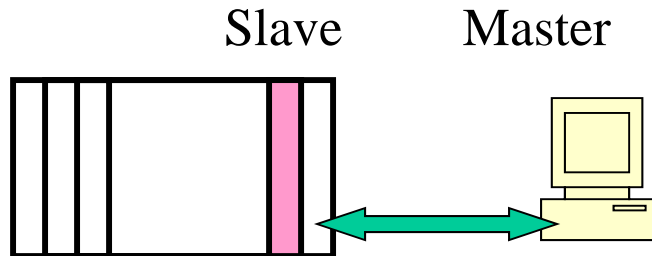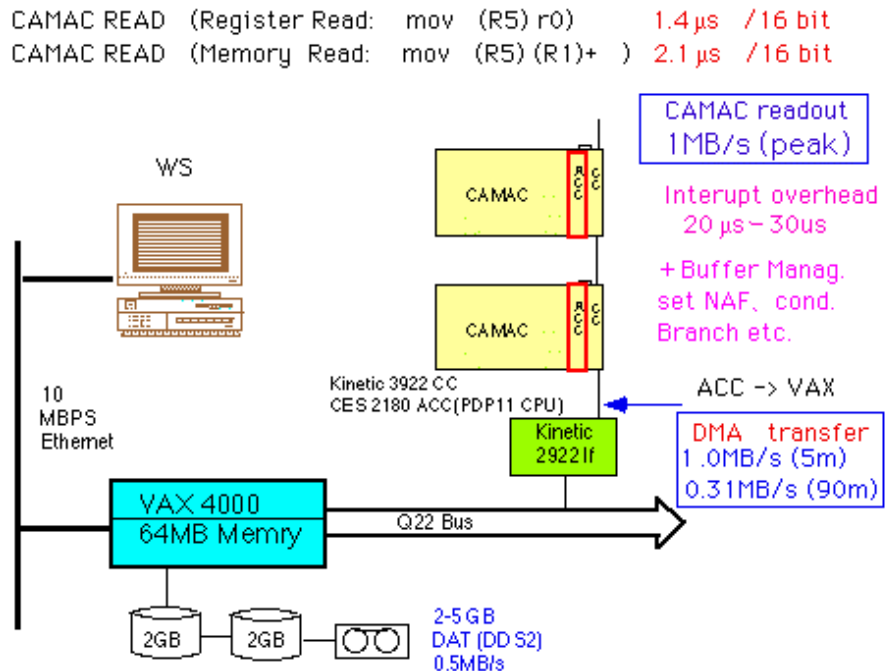- Serial Branch Highway: loop w/ two cables
- Parallel Branch Highway: thick cable, ~100 wires
- Peripheral Component Interconnect 32-b 33MHz
- Universal Serial Bus (2=480 Mbps, 3=5 Gbps)

All require appropriate adapter in CPU, slow because commands and data must travel up and down the line between computer and module through a crate controller.

Slave   Master

- Auxiliary crate controller: a (small) computer in the crate with a small program to collect the data into blocks and then transfer it out on command.

CAMAC READ   (Register Read: mov (R5) r0)   1.4 µs / 16 bit
CAMAC READ   (Memory Read: mov (R5) (R1)+) 2.1 µs / 16 bit

CAMAC readout
1MB/s (peak)

Interupt overhead
20 µs – 30us

+ Buffer Manag.
set NAF, cond.
Branch etc.

WS

CAMAC

CAMAC

Kinetic 3922 CC
CES 2180 ACC(PDP11 CPU)

Kinetic
2922 If

ACC -> VAX

DMA transfer
1 .0MB/s (5m)
0.31MB/s (90m)

10
MBPS
Ethernet

VAX 4000
64MB Memry

Q22 Bus

2GB   2GB

2-5 GB
DAT (DD S2)
0.5MB/s

T. Ichihara et al. IEEE Transaction on Nuclear Science, 36-5 p. 1628 (1989).

Data Acquisition: architectures – 2 –

Slave Master

CAMAC

VME

Parallel Branch

Ethernet

• Master/Slave concept with VME-based CPU's
   the NSCL daq system in the 1990's
   CAMAC modules do the work

(ANL 90's version)

CAMAC

VME

Parallel Branch

Optical Fiber (PCI/VME bridge)
Updated to USB connection
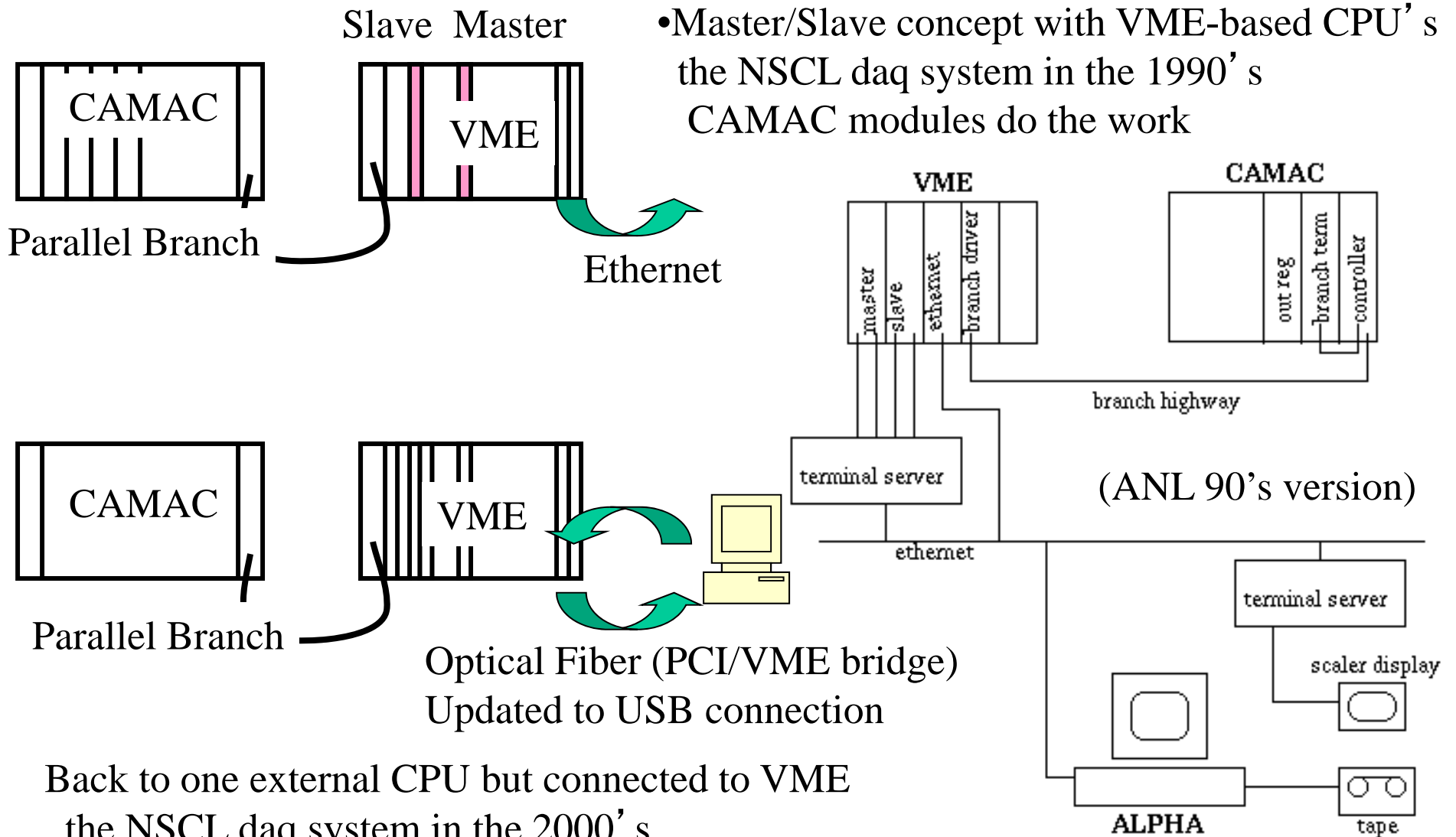
   Back to one external CPU but connected to VME
    the NSCL daq system in the 2000's
    VME modules are doing the work storing data in "external" memory
    CAMAC runs on a slower scale handled through a VME interface

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Distributed systems: MIDAS

MIDAS is an acronym for Maximum Integrated Data Acquisition System
https://www.psi.ch/ldm-no-computing/midas

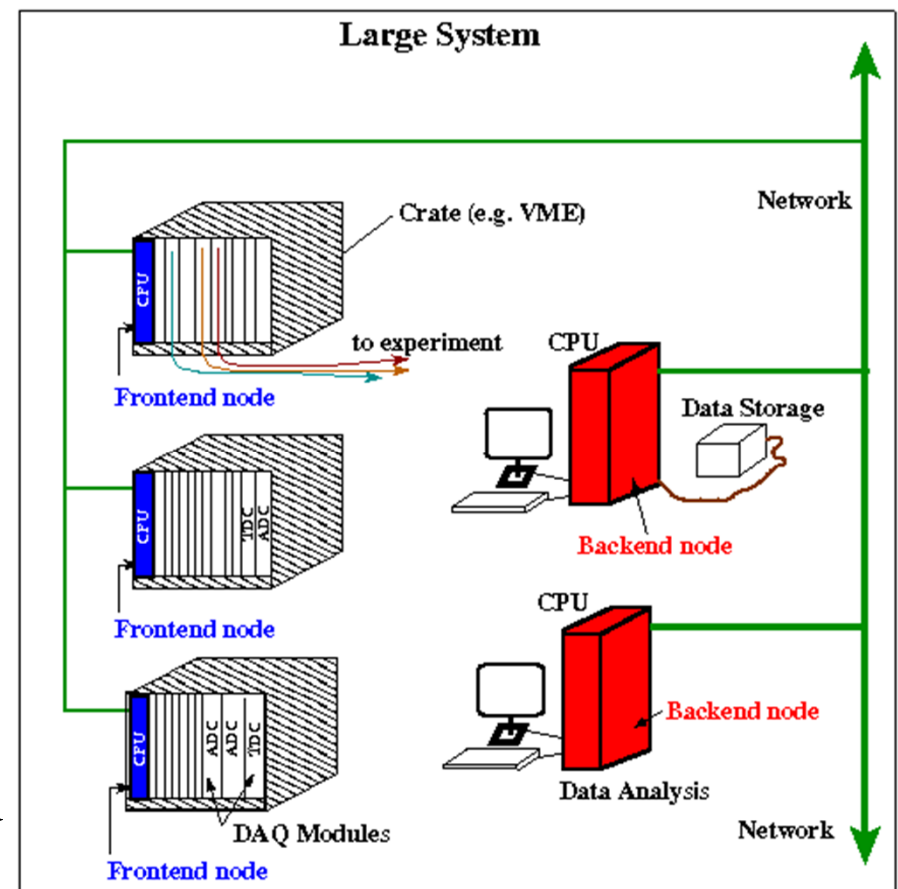- Back to the Master/Slave concept withVME-based slave CPU's (and new name) that do most of the work, CAMAC branch can be included, the Master sits on the Ethernet, can have as many lurkers as one wants on the net.

"Frontend" computers (slaves) acquire data from various hardware modules with direct access to the hardware, i.e., a computer running a dedicated program (app). For example, the CPU is programmed to read data from several TDC and ADC modules.
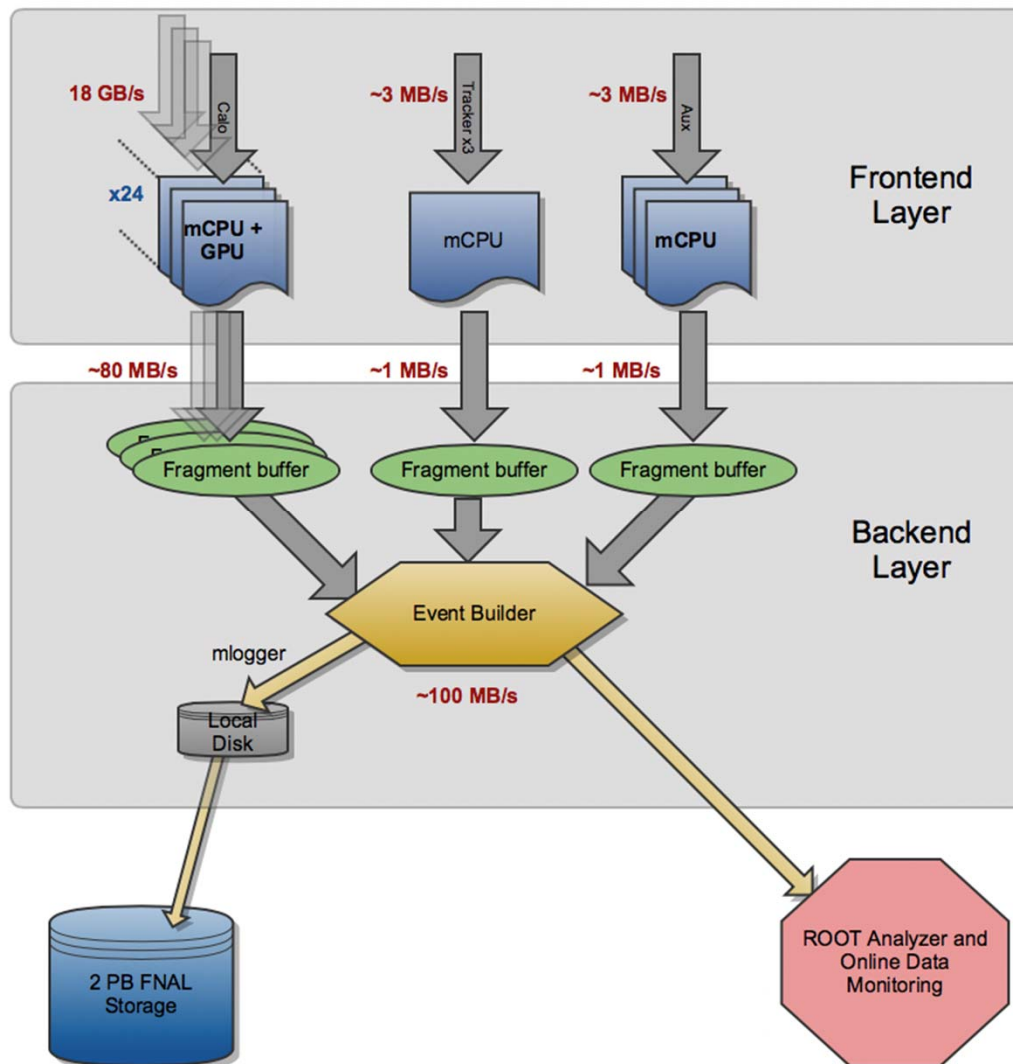
"Backend" computer(s) handle control/ storage and/or analysis of the data and receive data from one or more "frontends". Backend computer(s) may receive data from several frontends and build events based on time correlations (time stamps).

Time stamp is created by counting distributed clock pulses in scalers in each component.

Large System

Crate (e.g. VME)

Frontend node

to experiment

CPU

Network

Data Storage

Backend node

CPU

Backend node

Data Analysis

DAQ Modules

Frontend node

Network

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Distributed systems: g2 Expt.

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"The data acquisition system for this experiment must have the ability to record deadtime-free records from 700 µs muon spills at a raw data rate of 18 GB per second.

Data will be collected using 1296 channels of µTCA-based 800 MHz, 12 bit waveform digitizers and processed in a layered array of networked commodity processors with 24 GPUs working in parallel to perform a fast recording and processing of detector signals during the spill.

The system will be controlled using the MIDAS data acquisition software package."

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The GETINA data acquisition system that runs at the NSCL relies on counting clock pulses in scalers to synchronize separate data streams. The clock pulses occur every 10 ns and the scalers can count up to 2^{64} bits. What is the maximum time that this this system can run before the scaler times out?

The NSCL SeGA data acquisition system includes successive approximation ADC's (Ortec 413A's) that require approximately 10μs to complete the (parallel) conversion of all analog signals into digital words. The ADC's reside in CAMAC crates serviced by a code running in a LINUX computer (through PCI/VME and then VME/CAMAC interfaces). The time to store a data word from the module in the computer memory is approximately 8μs, assume other overhead times are negligible. (a) Estimate the dead-time per event if this system is used to readout an experiment that has ten parameters (ten data words). (b) Estimate the true rate and the fractional dead-time if this ten parameter experiment is running at the rate of 200 events/sec. (c) At what event rate will the system reach a fractional dead-time of 0.50 (at ten words/event)?
[Final Exam Question, F/2oo2]