Week 12: Chap. 18a Analysis (Acronym Day)

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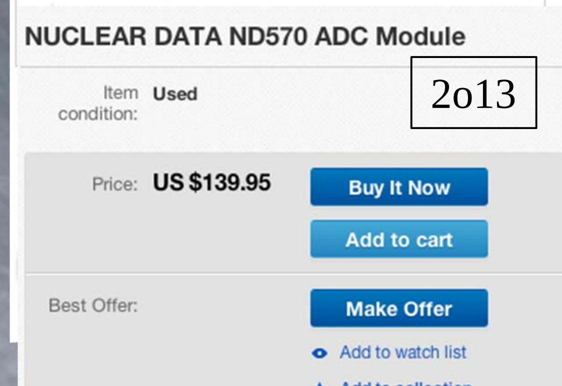
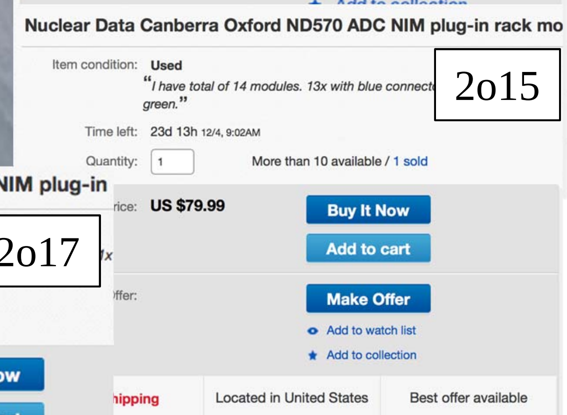
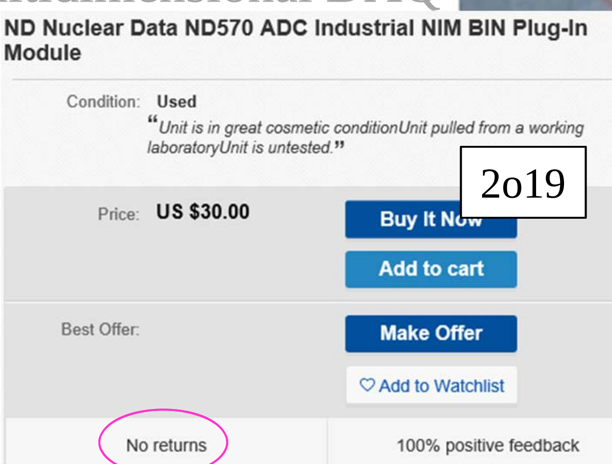
Pulse Processing

Analysis, A & T to D
-- Conversion time
-- Linearity
-- ADC types
--- Flash ADC
--- Sub-ranging
--- Successive Approximation
--- Wilkinson Ramp
-- Time to Digital

Analysis, Multidimensional DAQ







Final step in traditional pulse processing: convert analog (V) signal into a digital word.
[Third step in Digitial DAQ (detector, preamp, A to D Conversion)]

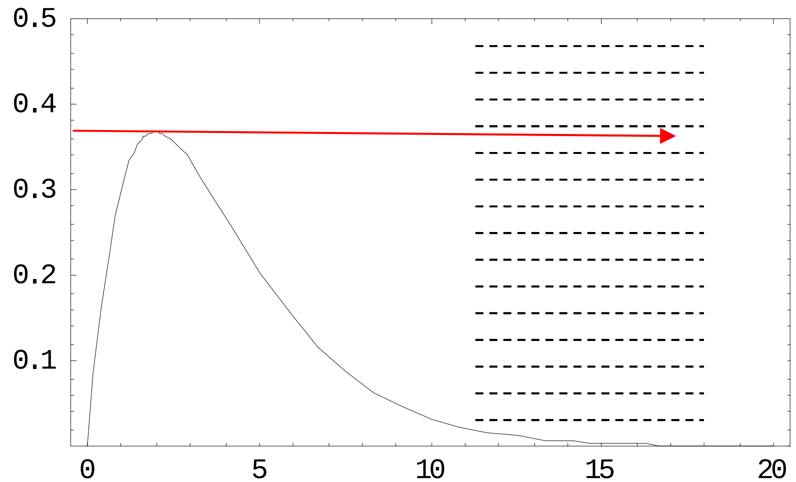
The input signal can be a voltage, charge, or time difference and is compared to a reference voltage (or charge) by a variety of techniques. The choice of comparison circuit (procedure) generally determines:

Resolution, Non-linearity (integral and differential), and Conversion time

Resolution: the resolution of an ADC is specified in terms of both the (voltage) range and the digital range (number of bits, N).

The voltage associated with the least significant bit (LSB), $V_{LSB} = (V_{max} - V_{min}) / 2^N$

Perfect device sorts the data into 2^N bins of equal width = 1 V_{LSB}



Example: V range = 0 to 0.5 V, 4-bit ADC
N=4, 2^N=16 V_{LSB}= 0.03125

Peak in bin #:
Decimal: 12 Binary: 1100, Hexadecimal: C

Analog to Digital: conversion time

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The input circuit can sometimes scale the input voltage signal into the accepted range.
The number of bins and the conversion time (or input rate limit) are generally linked.
The following table is from the manufacturer *Analog Devices* (www.analog.com)

Precision and General Purpose ADC Finder

Resolution (Bits)	ADC Throughput Rate (SPS)					
	<1K	1 - 100k	100 - 250k	250 - 450k	450k - 1M	1M - 10M
18 - 24	✓ (21)	✓ (22)	✓ (10)	✓ (10)	✓ (7)	✓ (6)
14 - 17	✓ (17)	✓ (17)	✓ (39)	✓ (22)	✓ (31)	✓ (29)
8 - 13	✓ (10)	✓ (13)	✓ (42)	✓ (12)	✓ (51)	✓ (61)

High-Speed ADC Finder

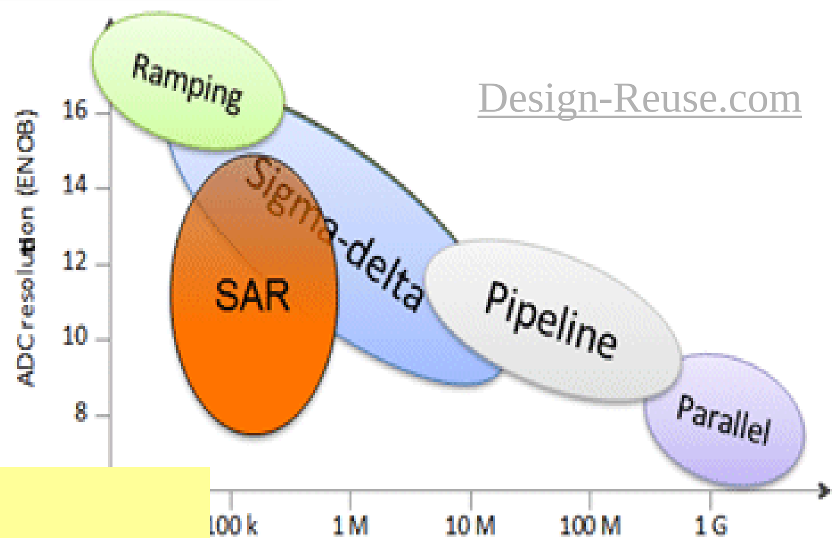
Resolution (Bits)	ADC Throughput Rate (MSPS)			
	10 - 50	50 - 100	100 - 250	250+
>/=16	✓ (12)	✓ (11)	✓ (14)	✓ (2)
14 - 15	✓ (16)	✓ (20)	✓ (27)	✓ (5)
12 - 13	✓ (31)	✓ (29)	✓ (29)	✓ (8)
10 - 11	✓ (13)	✓ (20)	✓ (23)	✓ (5)
</=9	✓ (5)	✓ (10)	✓ (9)	✓ (5)

~ 10^9 b/s

~ 1 ns/b

SPS – samples / second

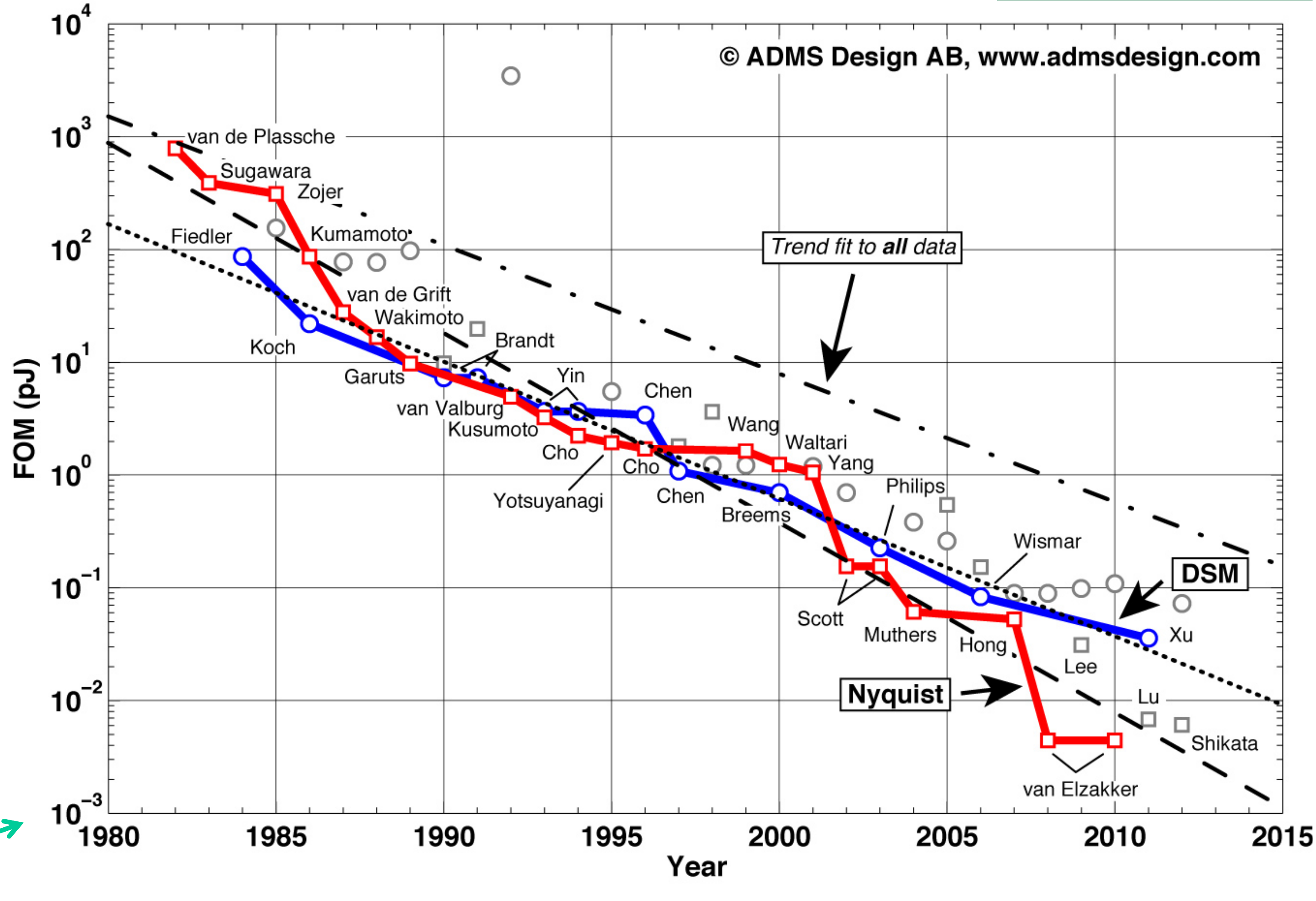
The algorithm used to convert the signal is generally correlated with the speed and resolution. Most modern devices (for sound, etc. processing) are used in a nearly continuous mode, rather than in a pulse processing mode.



Typical Nuc Phys Hi Res device 13b/6 μs ~ 2x10^6 b/s
Typical "digital electronics" device 12b@100MHz ~ 1x10^9 b/s

Analog to Digital: aside on ADC history

Figure of Merit is Power (pJ) "on Chip" needed to process event

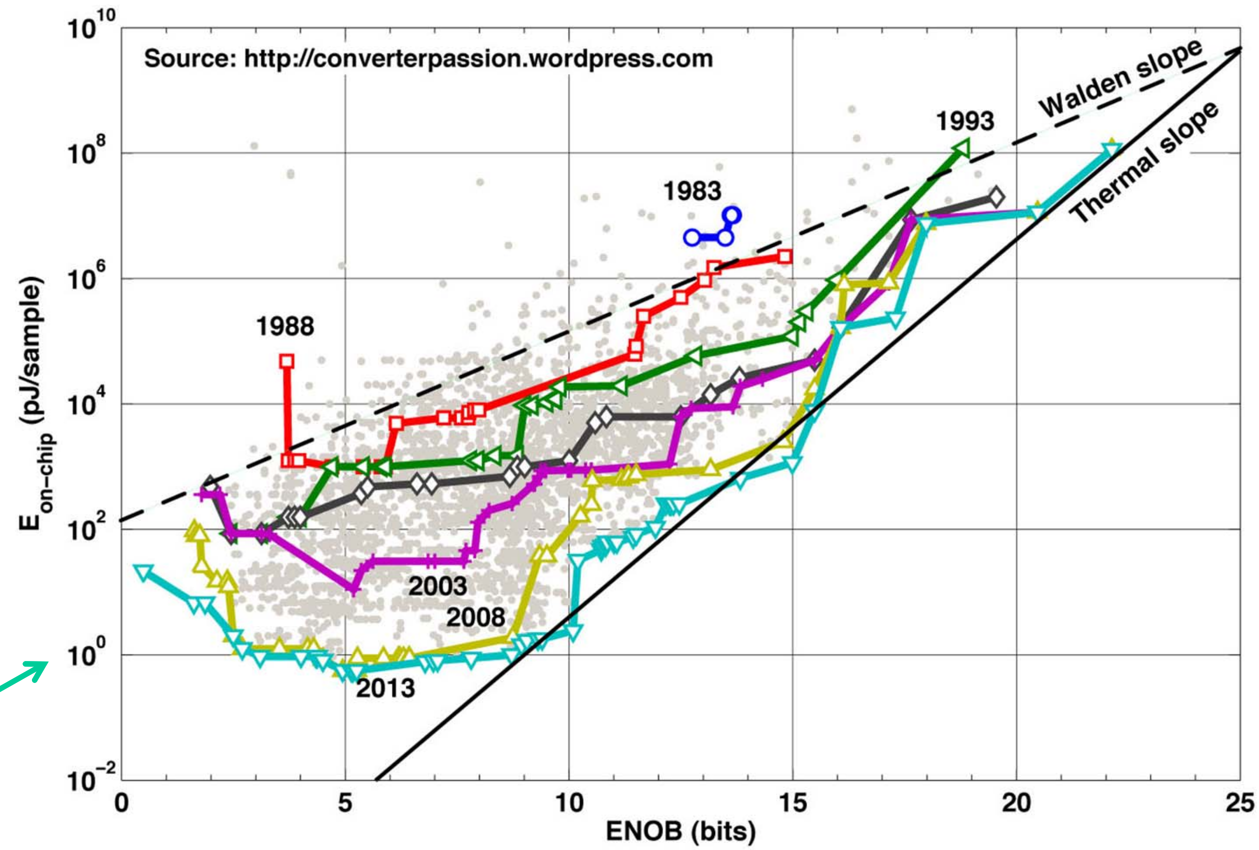


10^{-15} J / 1.6×10^{-19} J/eV = 6.2×10^{3} eV

DSM – Delta-Sigma Modulation
Nyquist – frequency sampling device

Analog to Digital: aside on signal size

Power (pJ) "on Chip"
needed to process event



Presently a "plateau" near:
10^{-12} J / 1.6×10^{-19} J/eV = 6.2×10^{6} eV

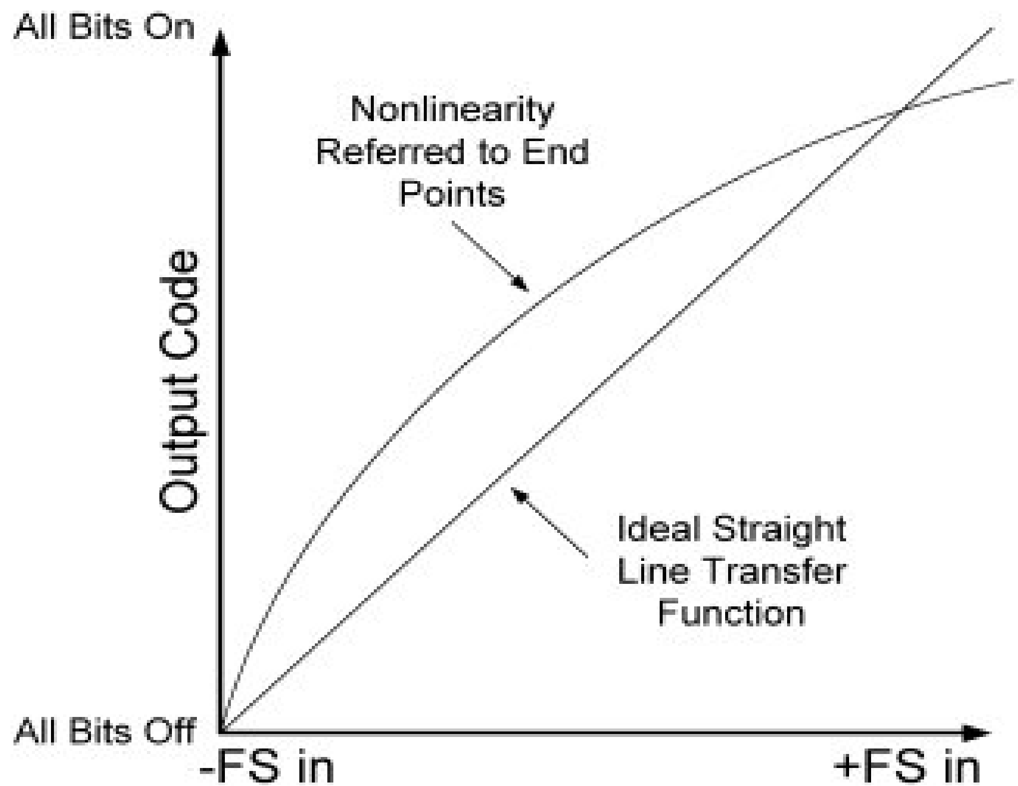
"Effective Number of Bits"
= $\mathrm{Log}_2\,[V_{\mathrm{FullScale\ In}} / (f * V_{\mathrm{ADC\text{-}RMS\text{-}Noise}})\,]$

Thermal slope from shot-noise variation with power
Walden slope is an empirical rule.

Analog to Digital: Linearity

The devices are expected to be linear – thus the small deviations are quoted in terms of the integral and differential **non-linearity** (INL & DNL).

$$\text{INL} = [(V_D - V_0) / V_{LSB}] - \text{DataWord}$$

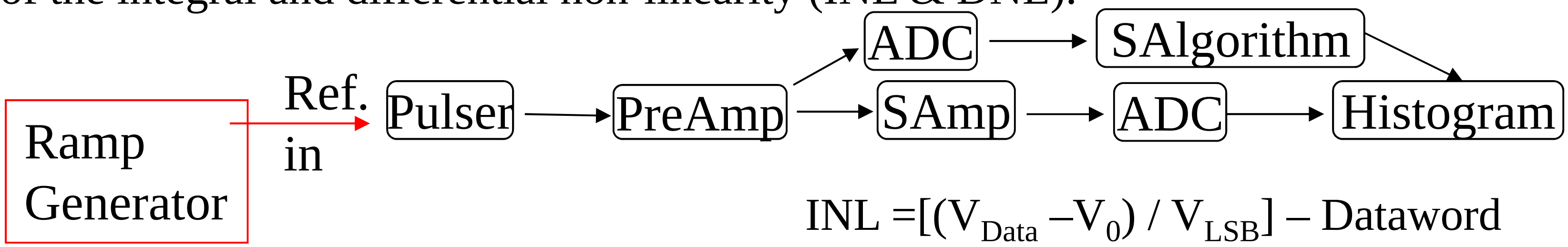


See alternate version:

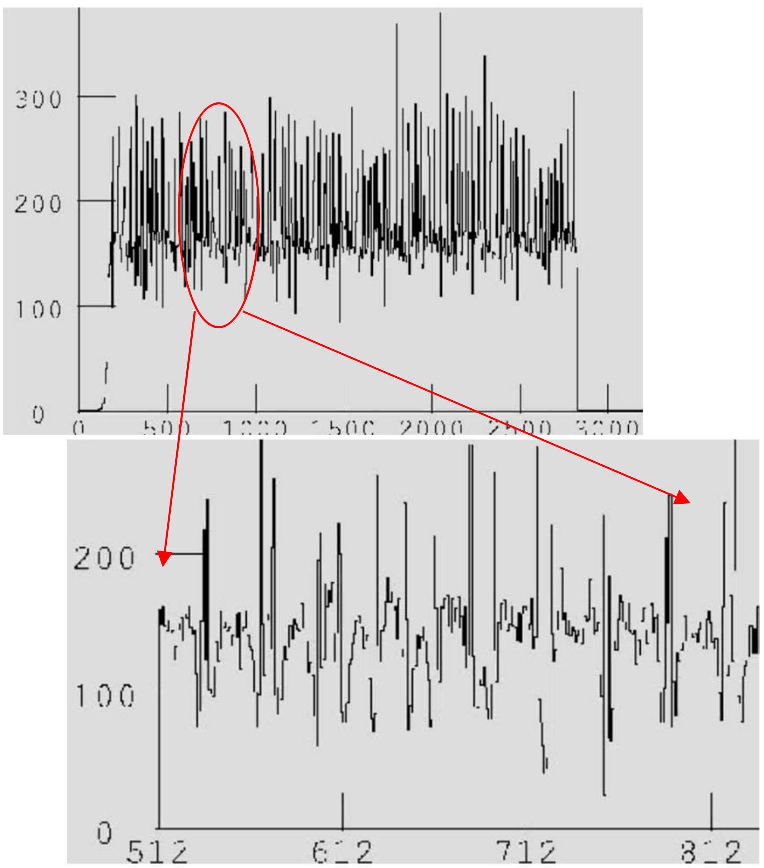
Fig. 18.6 Knoll, 3rd, 4th Eds.

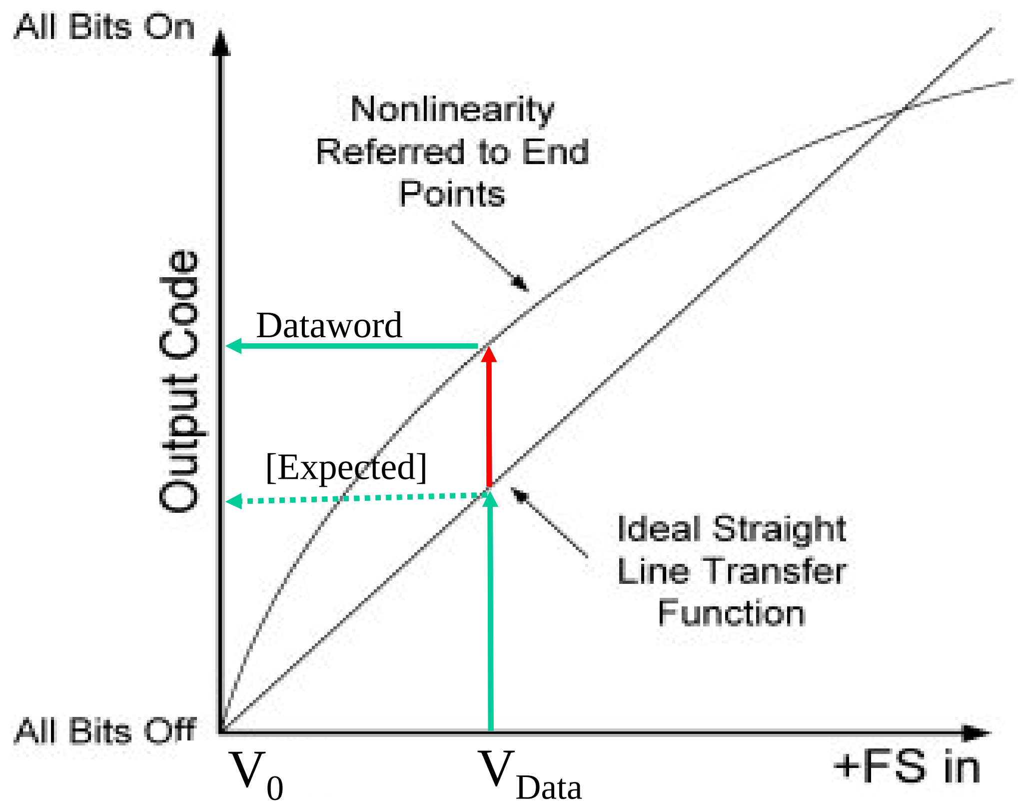
Analog to Digital: Linearity

The devices are expected to be linear – thus the small deviations are quoted in terms of the integral and differential non-linearity (INL & DNL).



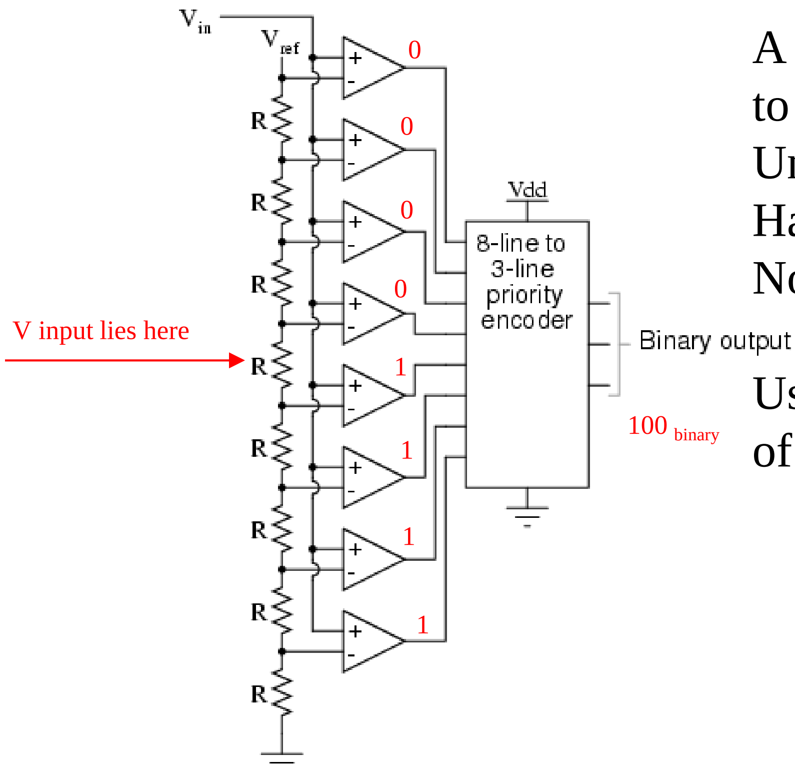
$$INL = [(V_{Data} - V_0) / V_{LSB}] - \text{Dataword}$$





$$DNL = (\Delta V_i / V_{LSB}) - 1$$

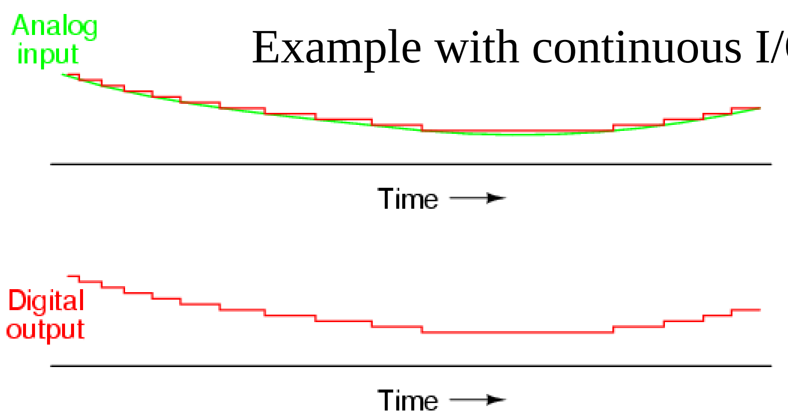
Analog to Digital: Flash ADC



A Flash ADC is the fastest device: the input is compared to a set of reference voltages simultaneously.
Uniform conversion time.
Hardware intensive: 2^N comparators
Nonlinear: resistor chain & comparators can vary

Use in nuclear physics growing, digital signal recording of the pulse waveform (aka: trace)

Example with continuous I/O



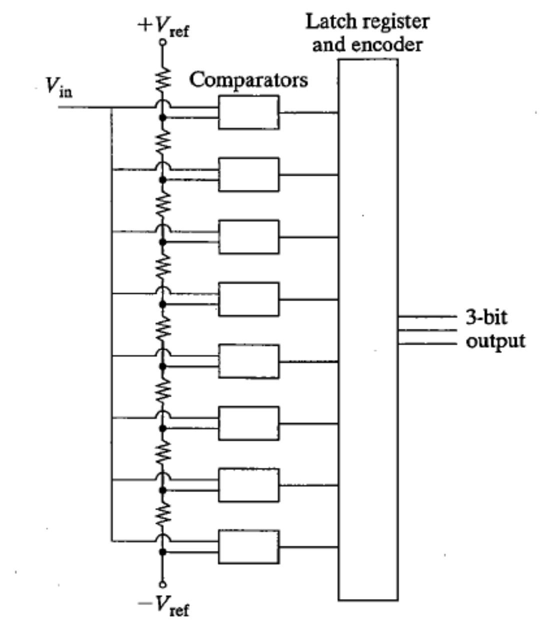
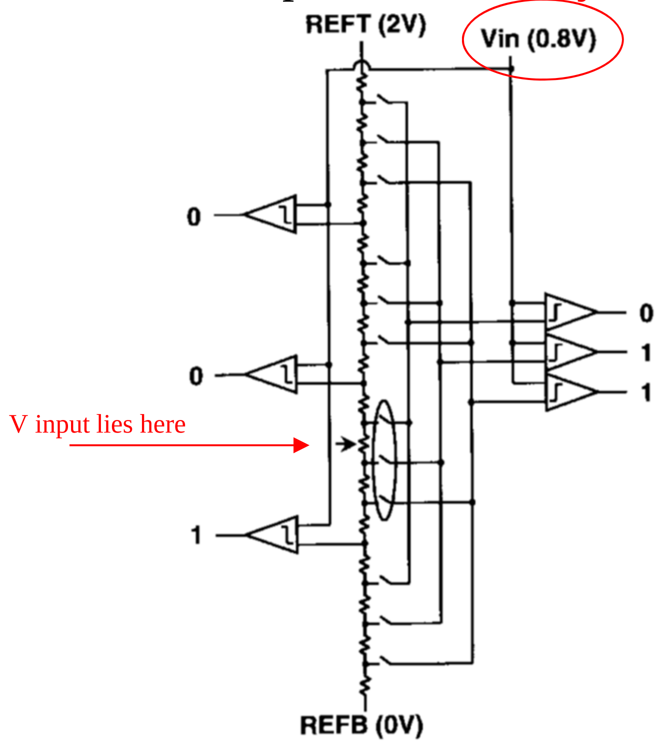


Fig. 17.31 Knoll, 3rd Ed.

17.42 in 4th Ed.

Analog to Digital: sub-ranging ADC

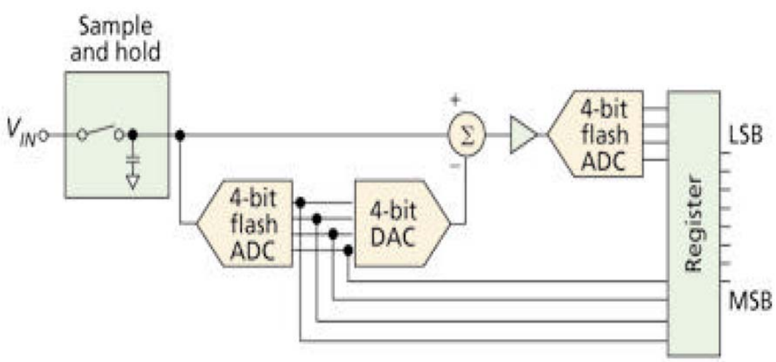
Caution: Example is not Binary Encoding



A sub-ranging ADC compares the input signal to the voltage on a resistor chain using several banks of comparators in sequence.

Uniform conversion time.
Hardware requires switching banks several comparators
Linearity & Resolution again limited by resistor chain and comparators

Example with Binary Output (16 resistors in chain):
V_{LSB} = 2V/16bits = 0.125 V
0.8 V (2V range) $\rightarrow$ 40% (FS is 2^4)
0.4 * 16 = 6.4 , expect $6_{decimal}$ = 0110_{binary}



Alternate device determines the upper range and then subtracts it away with a DAC signal … 15 comparators in the subranging ADC to process the signal compared to 2^8 comparators in an 8-bit flash ADC.

Analog to Digital: successive approximation

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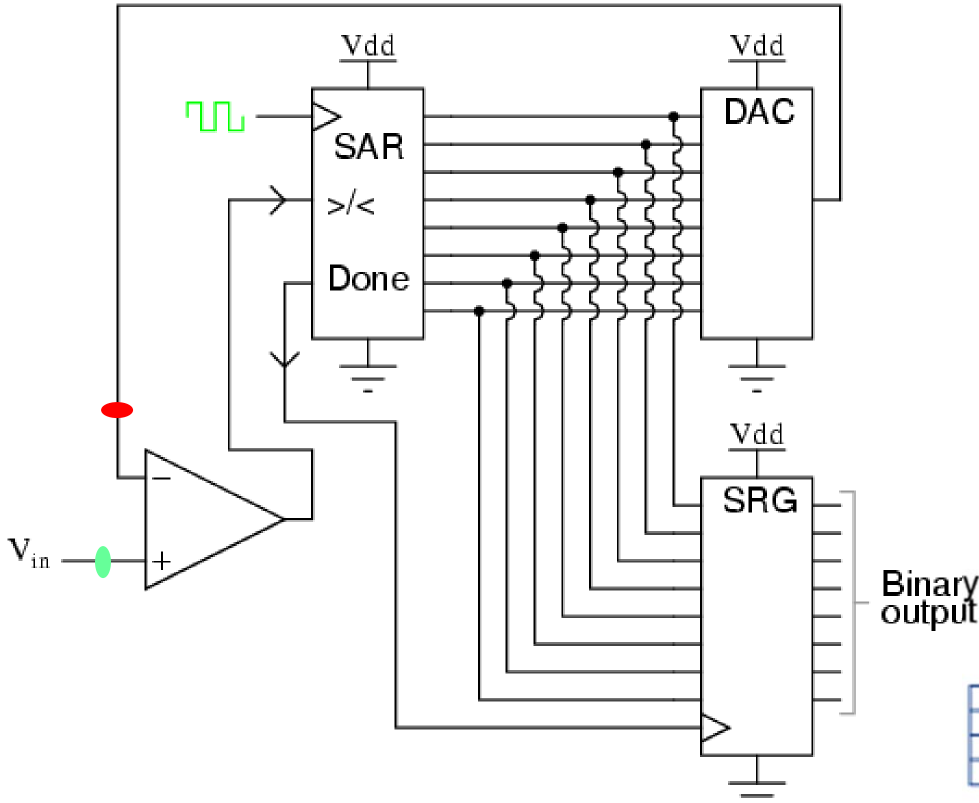
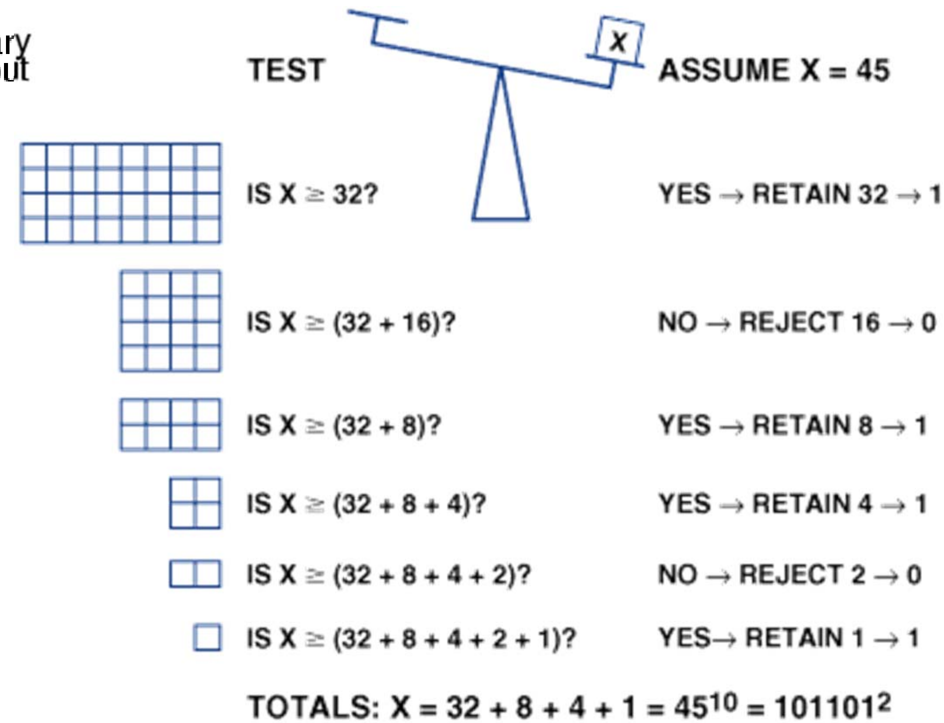
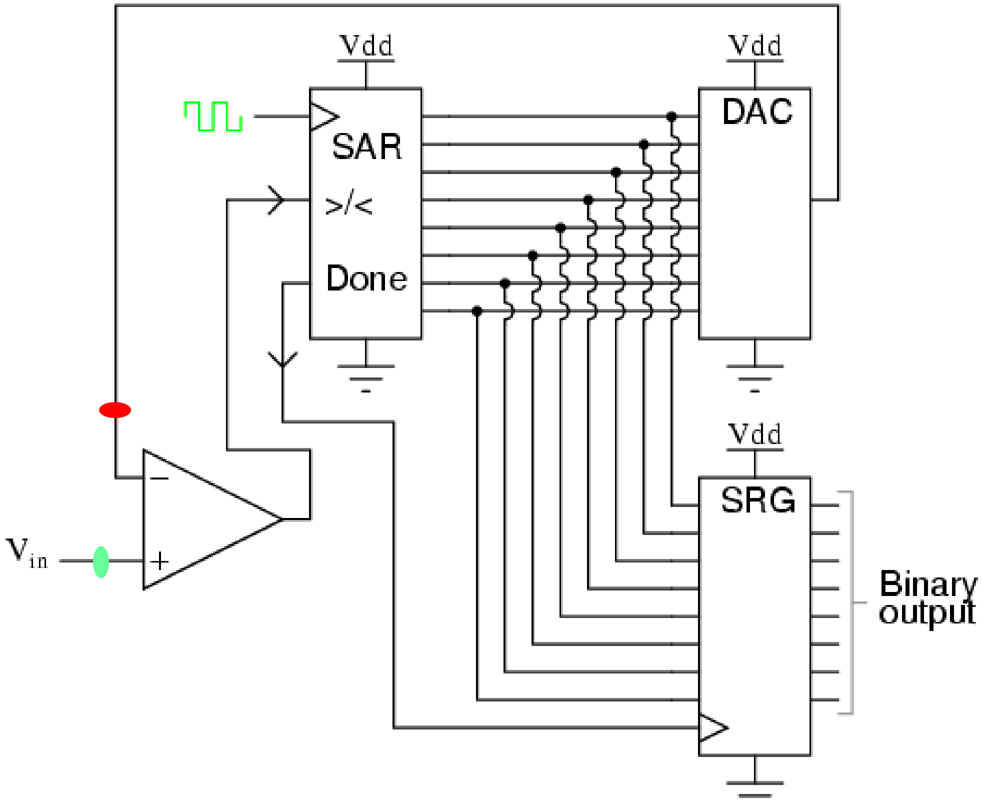


A successive-approximation ADC compares the input signal to a digitally generated signal (usually) starting at the midpoint of the range.

DAC output



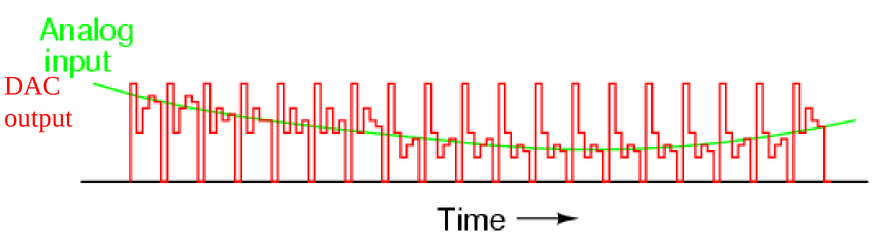
Analog to Digital: successive approximation



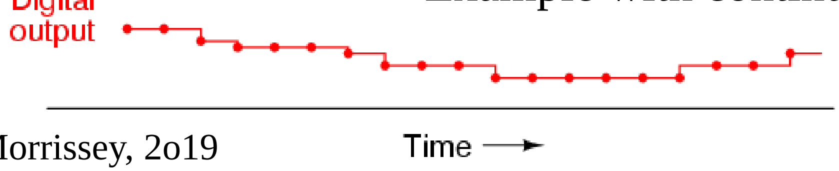
A successive-approximation ADC compares the input signal to a digitally generated signal (usually) starting at the midpoint of the range.

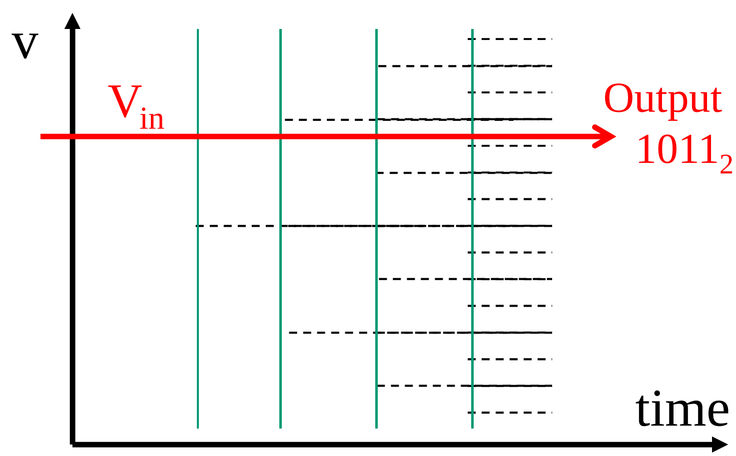
Uniform conversion time.
Hardware requires accurate DAC
Linearity: one comparitor and one DAC
Resolution usually limited by DAC

Very common in nuclear physics but not for the highest resolution systems.



Example with continuous I/O





Analog to Digital: Wilkinson Ramp ADC

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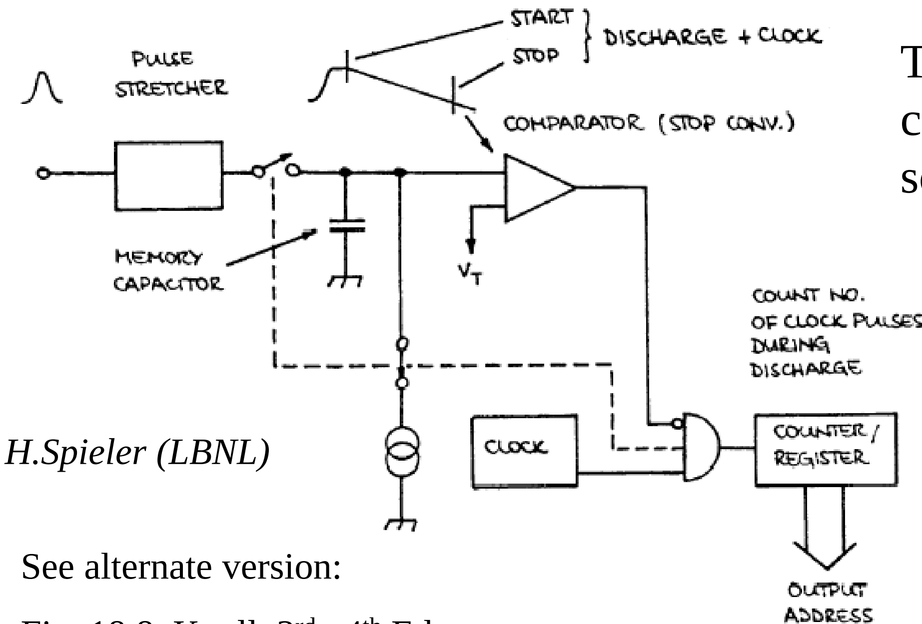


H.Spieler (LBNL)

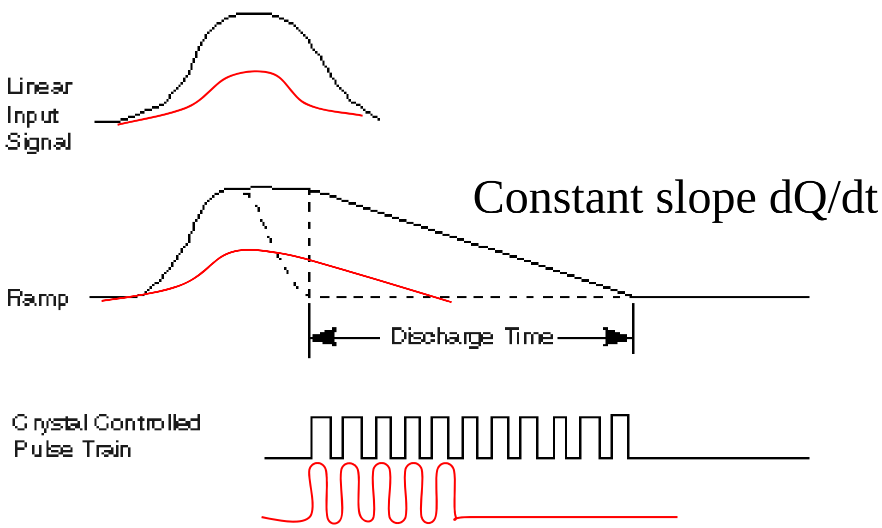
See alternate version:

Fig. 18.8 Knoll, 3rd , 4th Eds.

The input signal is stored as a charge on a capacitor that is discharged by a constant current source with a clock (100 up to 400 MHz)

Variable conversion time.
Linearity: one comparitor but stretcher
Input rate limited by clock rate

Used for highest resolution devices in nuclear physics, i.e., Ge detectors.



8192 /400 MHz ~ 20 μs

Analog to Digital: the Gatti Register

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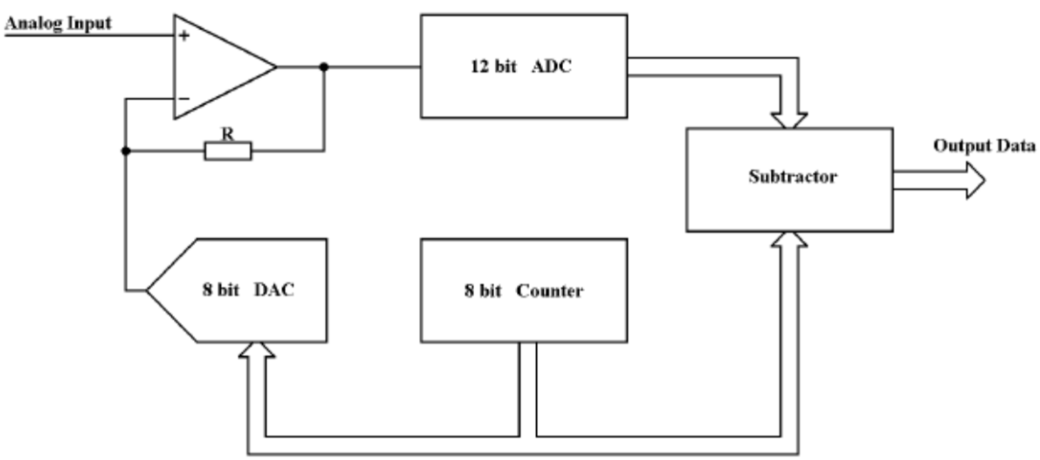
The highest resolution ADC's generally over-sample the signal using a technique based on the "Gatti Register" or sliding-scale register [Cottini, Gatti, & Svelto NIM 24(1963)241] to improve the differential non-linearity by averaging the response of the ADC. The idea relies on application to large sets of measurements of the same signal (e.g., peaks in spectra). There is no free lunch, the averaging results in a loss of some dynamic range.

One example of many variations:



R.Bassini, et al. (InFN-Milano) See alternate version:

Fig. 18.10 Knoll, 3rd , 4th Eds.

Example: 2^{12} = 4096 channels
2^{8} = 256 channels
Values in range 3840-4096 not valid!

- The counter contains a random number and generates a voltage that is added to the input voltage.
- The analog signal is converted to a larger number but the value of the counter is then subtracted.
- The counter is incremented before the next pulse.

The net effect for many pulses is to smear out the DNL.

N.B. The voltage step of each bit in the DAC must be exactly equal to the step size (LSB) in the ADC.

Analog to Digital: time to digital

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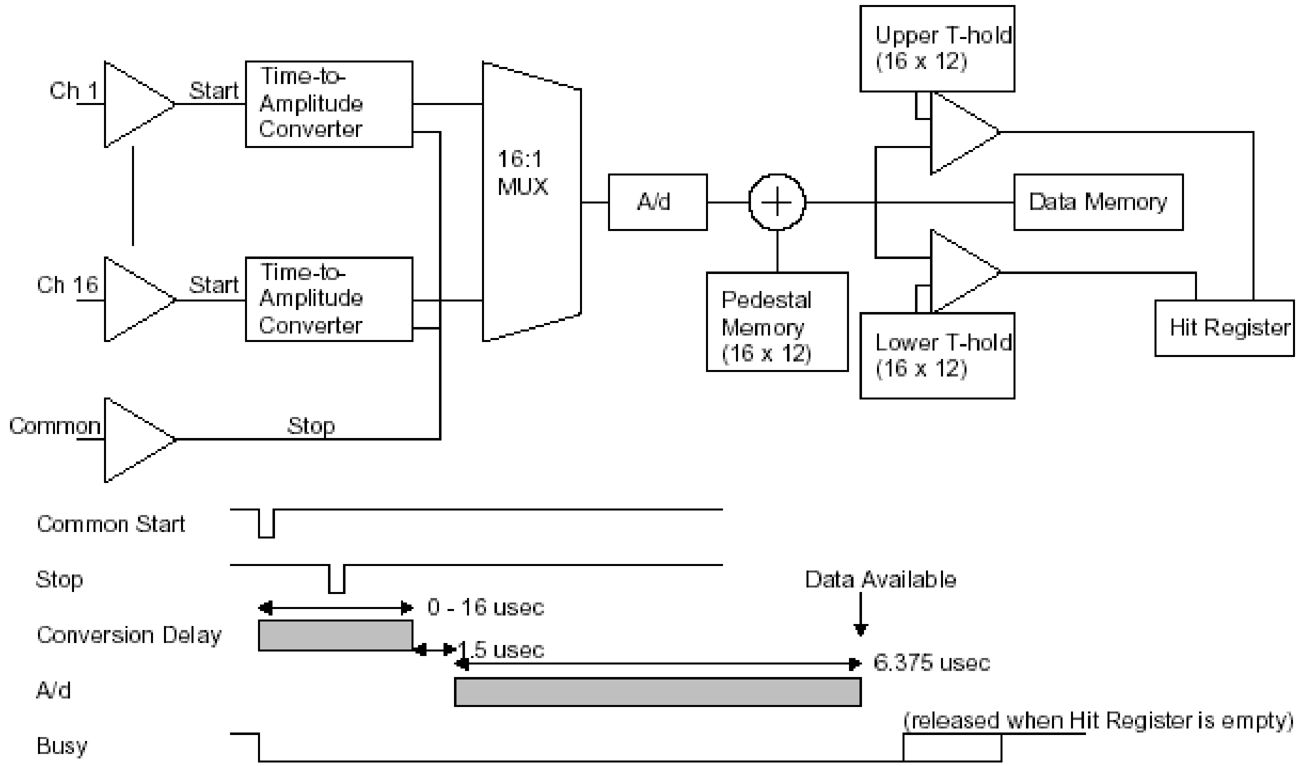
Time differences are recorded in two ways:

•Creation of an amplitude signal from the time difference followed by a “normal” ADC

Phillips Scientific 7186



•Counting clock pulses between start/stop signals – generally limited to Δt =1 ns or poorer resolution, can read multiple hits before & after start (with appropriate logic)
AKA – multihit TDC

Chap. 18a – Analog to Digital: question

Problem 18.11 – The following data is part of a gamma-ray pulse height spectrum. It can be assumed that the data consist of a constant background plus a Gaussian peak.

a) Plot the data, estimate the constant background level, find the net number of counts, estimate the centroid and FWHM.

b) Fit the data with a Gaussian function …

Problem 18.10 – Plot the second derivative of .. (the data).

Ch No	Cts
711	238
712	241
713	219
714	227
715	242
716	280
717	409
718	736
719	1190
720	1625
721	1739
722	1412
723	901
724	497
725	308
726	256
727	219
728	230

Problem 18.11 – The following data is part of a gamma-ray pulse height spectrum. It can be assumed that the data consist of a constant background plus a Gaussian peak.

a) Plot the data, estimate the constant background level, find the net number of counts, estimate the centroid and FWHM. [N.B. this was done by the computer for you in PS#3]

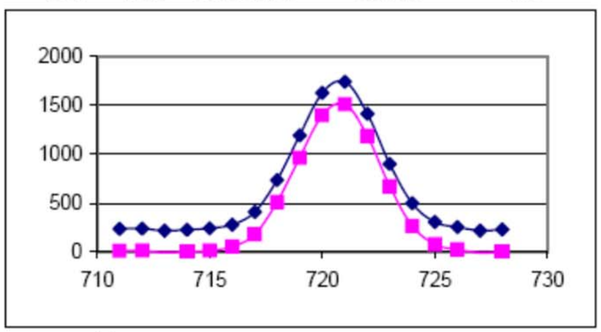
b) Fit the data with a Gaussian function …

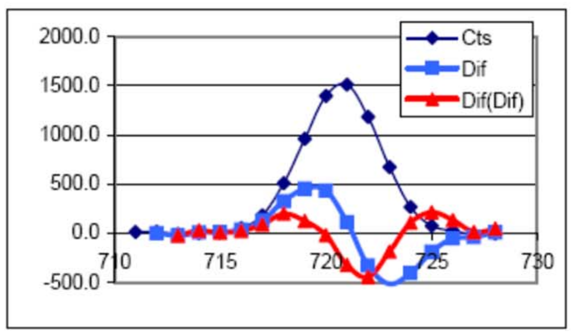
Problem 18.10 – Plot the second derivative of .. (the data).

Ch No	Cts	Sqrt(Cts)	Bkg	Cts-Bkg				Dif	Dif(Dif)
711	238	15.42725	224.5	13.5	Sum(715/727)	9595.00	97.95		
712	241	15.52417	224.8	16.2	N_chan	12.00		2.7	
713	219	14.79865	225.1	-6.1	Avg_Lo	229.00		-22.3	-25.0
714	227	15.06652	225.3	1.7	Avg_Hi	224.50		7.7	30.0
715	242	15.55635	225.6	16.4	Avg_BKG	226.75		14.7	7.0
716	280	16.7332	225.9	54.1	N*Bkg	2721.00	52.16	37.7	23.0
717	409	20.22375	226.2	182.8	Sum-N*Bkg	6874.00	110.98	128.7	91.0
718	736	27.12932	226.5	509.5	SumCh	12951.00		326.7	198.0
719	1190	34.49638	226.8	963.3				453.7	127.0
720	1625	40.31129	227.0	1398.0	Centroid	720.64		434.7	-19.0
721	1739	41.70132	227.3	1511.7	Width	2.24		113.7	-321.0
722	1412	37.57659	227.6	1184.4				-327.3	-441.0
723	901	30.01666	227.9	673.1	X-bar	720.69		-511.3	-184.0
724	497	22.2935	228.2	268.8	sigma	1.80		-404.3	107.0
725	308	17.54993	228.4	79.6				-189.3	215.0
726	256	16	228.7	27.3				-52.3	137.0
727	219	14.79865	229.0	-10.0				-37.3	15.0
728	230	15.16575	229.3	0.7				10.7	48.0

$$\overline{Centroid} = \sum_{711}^{728} N_i * i \Big/ \sum_{711}^{728} N_i$$

$$Width^2 = \sum_{711}^{728} (i - \overline{Ch})^2 N_i \Big/ \sum_{711}^{728} N_i$$





Chap. 18a – Analog to Digital: question, too

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Estimate the minimum conversion time for an Ortec AD811 ADC to convert a 1 V pulse.

The AD811 Octal ADC contains eight peak-measuring analog-to-digital converters packaged in a single-width CAMAC module. The instrument is designed to measure positive unipolar or bipolar signals from nuclear shaping amplifiers in the range of 0 to +2 V. The device uses the Wilkinson technique with a 50 MHz clock. The AD811 provides 1 mV resolution with a range of 11 bits (2047 counts) and a 12th bit is included in each of the eight data registers for overflow detection.

What is V_{LSB} and the conversion time per bit for an Ortec *AD413A* ADC ?

The *AD413A* ADC contains four peak-measuring analog-to-digital converters packaged in a double-width CAMAC module. The instrument is designed to measure positive signals from shaping amplifiers in the range of 0 to +10 V. The device uses the successive approximation technique with a 6 μs conversion time for 13 bits.