Chemistry 985

Fall, 2o19 Problem Set #5
Distributed: Tues., 12 Nov. 2019 Due: Tues., 26 Nov. 2019

Show your work! Indicate sources of external data!

1. S/N
   The lab has a few high-gain charge sensitive preamplifiers that can be set to an output gain of 1.00 V per 100 MeV of deposited charge. What are the ENC and S/N ratio for the most intense alpha particle from ^{249}Cf decay for one of these preamps if the white noise was found to be 12 mV?

2. Constant Fractions
   A signal from a silicon preamp is sent to a timing-filter amplifier (TFA) with time constants (τ CR/RC = 50/50 ns) leading to a typical amplitude of 1.0 V and an RMS noise of 10mV and then to a Phillips 715 CFD.

   (a) What is the appropriate length of delay cable for this CFD?

   (b) What is the expected timing resolution for this channel?

3. ADCs
   The following text was cut from the user manual of the Caen V785 32-channel peak sensing ADC. What is V_{LSB} and the range of valid voltage inputs (the minimum and maximum values) that will result in a valid digital output when this module is operated with the Gatti "sliding scale" register and a lower level threshold of 255_{10} or 0xFF set appropriately in memory?

   The Model V785 is a 1-unit wide VME 6U module housing 32 Peak Sensing Analog-to- Digital Conversion channels. Each channel is able to detect and convert the peak value of the positive analog signals (with >50 ns risetime) fed to the relevant connectors. Input voltage range can be 0 - 4 V. The outputs of the PEAK sections are multiplexed and subsequently converted by two fast 12-bit ADCs (5.7 μs for all channels). The ADCs use a sliding scale technique in order to reduce the differential non-linearity. Programmable zero suppression, multievent buffer memory, trigger counter and test features complete the flexibility of the unit.

   ... The peak values, received from the channel inputs when the GATE input signal is active, are converted into voltage levels by the Peak Sensing sections and then multiplexed and converted by two fast 12-bit ADC modules. Only the values that are above a programmable threshold and do not cause overflow will be stored in a dual port data memory for readout accessible via VME.

   ... The ADC section supports the sliding scale technique to reduce the differential non-linearity [1], [2] using an 8 bit counter. This technique (see Fig. 2.4) consists in adding a known value to the analog level to be converted, thus spanning different ADC conversion regions with the same analog value. The known level is then digitally subtracted after the conversion and the final value is sent to the threshold comparator.

... The output of the ADC is fed to a threshold comparator to perform the zero suppression. If the converted value from an input is greater than (or equal to) the relevant low threshold value set via VME in the Thresholds memory (located at Base Address + 0x1080 to 0x10BF), the result is fed to the dual port memory and will be available for readout.

[1] C. Cottini, E. Gatti, V. Svelto, A new method of analog to digital conversion, NIM vol. 24 p.241, 1963.

[2] C.Cottini,E.Gatti,V.Svelto, A sliding scale analog to digital converter for pulse height analisys, in Proc. Int. Symp. Nuclear, Paris, Nov. 1963.

4. Data Stream
   The following hexadecimal words were found as part of the data stream from a recent experiment using digital data acquisition and a 100 MHz PIXIE-16 module. Decode the first event using the information in Table 4-2, etc. of the PIXIE-16 user manual. Indicate the decimal (base 10) channel number, event time_LO, event time_HI and event energy for the first event.
   00044113x 00ABD843x 800004D2x 80000406x 0004411Dx 00ABFF3x ...