UNIT 6 Logic Gates, Flip-Flops, and Counters

Chemistry 838

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Name	
Student Number	
Date Submitted	

Table of Contents

1. Instructions

1.1. General

This unit contains background information, a series of procedures for you to do, observations for you to make, and questions for you to answer.

The procedures that you are to perform and the observations that you are to make are contained in shaded boxes such as the following. In some cases you are provided tables in this document in which you may record the results of these observations. Alternatively, you may elect to record all information on separate pages. If you use separate pages, be sure to annotate everything with the procedure numbers so that you may easily correlate your information with the Unit at a later time.

Procedure 0:   Locate the oscilloscope and connect to the circuit in the figure. Sketch the output, being sure to label your drawing so that you can quantitatively determine the attributes of the signal observed.

Any analysis of the data, any further presentation of the data and the questions that you are to answer are presented in shaded boxes as below.

Question 0:   Transcribe the plot of the signal from the previous procedure to your report. What is the amplitude of that signal?

The Procedure and Question above are examples and are not to be included in this unit.

1.2.   Report Format

The report for this unit will consist of the following.

1. This document with your name, PID, and date of submission in the appropriate place on the first page of the document. In addition, all of your data is to be entered in the appropriate locations in the document.

2. Attach a separate document containing your answers to the questions arranged in order and identified as to question number.

3. Staple all the parts of your report together.

Alternatively, your may create a separate document that contains the following.

1. The first page with your name, PID, the title "CEM 838 Unit 6," and date of submission.

2. All of your recorded data transcribed into the document and identified as to Procedure and/or table number.

3. Your answers to the questions arranged in order and identified as to question number. You may interlace these with the procedures if you desire, but maintain the order of the original Unit 6 document.

4. Staple all the parts of your report together.

2. Introduction

The NAND, NOR, and Exclusive-OR logic gates in the famous 7400 series TTL family of integrated circuits are studied first in these experiments. Various combinations of these basic inverting logic gates are shown to provide important comparator, adder, multiplexer, and decoder operations. Flip-flops are combined to form counters and an IC up/down counter is connected and operated in conjunction with a versatile counter input gate.

3. Basic Logic Gates

Objectives: To introduce the inverting gates, NAND, NOR, and AND-OR-INVERT (AOI). Also, to demonstrate how equivalent logic functions can be achieved with either NAND or NOR gates by observing the tables of states for the inverting gates and the equivalent tables of states for equivalent functions.

Procedure 1:   Install the basic gates job board connecting the necessary power.

There are two types of NAND gates on the Basic Gates Job Board. The 7400 chip contains four, 2-input NAND gates (See Figure 1) while the 7420 has two, 4-input gates (See Figure 2). The layout of the signals, i.e. the pin outs, is documented in the figures contained in the Appendix (Section 10.3. TTL IC Pin Outs).
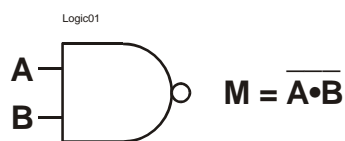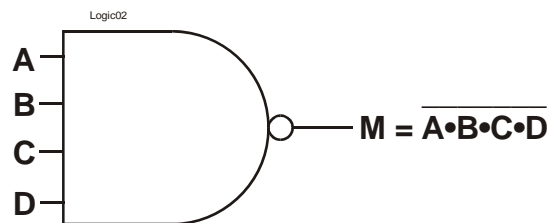

Logic01

$$A$$
$$B$$
$$M = \overline{A \bullet B}$$

Figure 1

Logic02

$$A$$
$$B$$
$$C$$
$$D$$
$$M = \overline{A \bullet B \bullet C \bullet D}$$

Figure 2

Procedure 2:   Use four of the switches in the Digital Output section of the Mini-Lab 200 (See Figure 28 in the Appendix) as inputs, and the Digital Indicators of the Mini-Lab 200 as indicators to verify the table of states for one gate on each chip and report the results. Also use the DMM to observe the voltage of the output for each state. Don't forget to provide power and ground to all job boards and all chips that you utilize. Record your observations in Table 3. Since this is a table of states for a device, the data should be recorded as LO and HI, not as 1 and 0. The latter is an arbitrary assignment not inherent in the device.

Question 1:   For the 2-input NAND gate, rewrite the table of states observed using 1 for LO and 0 for HI. This is now the truth table for the logic function performed by the gate on LO-true signals. What is the function?

Table 1

7400 Gate			
Inputs		Output	
A	B	$M = \overline{AB}$	voltage
L	L		
L	H		
H	L		
H	H		

Table 2

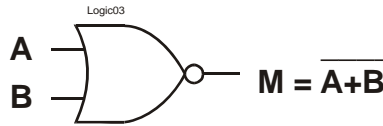| 7420 Gate				
Inputs				Output
A	B	C	D	$M = \overline{ABCD}$

Table 3

$$M = \overline{A+B}$$

Figure 3

Procedure 2: Similarly, investigate the table of states for the 7402 quad, 2-input NOR gate shown in Figure 3.

Table 4

7402 NOR Gate		
Inputs		Output
A	B	$M = \overline{A+B}$

Question 3: For the 2-input NOR gate, write the truth table (1's and 0's) for the response observed for LO-true signals. What is the function performed?

Question 4: If a NAND or NOR gate is available and the inverter function is needed, how would you connect the gate to achieve this function?

Question 5:   In a chemical process it is desired to sound a warning buzzer under the following conditions. The pH of the reaction mixture is outside the range pH 4-8 <u>and</u> the temperature of the mixture exceeds 50°C <u>or</u> the stirring motor is not turning and the temperature exceeds 30°C. The following signals are available.

1.   pH sensor output (analog)

2.   Temperature sensor output (analog)

3.   Stirring motor ON signal (logic level)

Use analog comparators and logic gates to generate a logic level signal that is HI when the warning buzzer should sound and LO when it should not. Show the circuit and the truth table.

Question 6:   All the basic gate functions can be performed by one type of inverting gate. Often it is convenient or economical to use one type of gate for all the required logic functions. Show that the three AND gate circuits in Figure 4, Figure 5, and Figure 6 are equivalent and the two OR gate circuits in Figure 7 and Figure 8 are equivalent. Logical equivalence is demonstrated by identical tables of states or may be shown using Boolean algebra.

Do not wire these circuits.

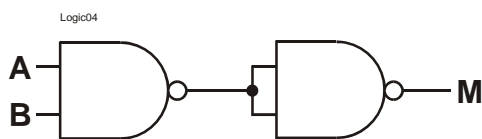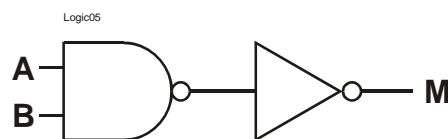Table 5 and Table 6 are provided for recording your data. Transcribe these tables into your report.
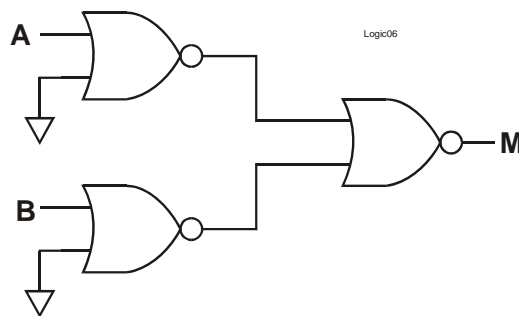
Logic04

Figure 4

Logic05

Figure 5

Logic06

Figure 6

Table 5

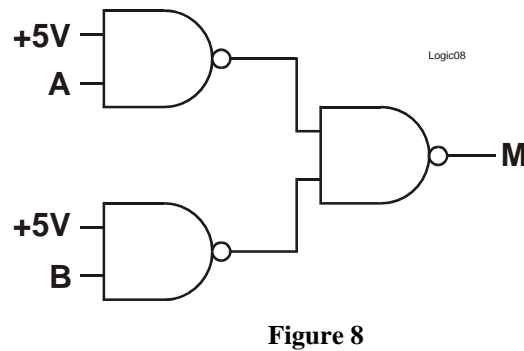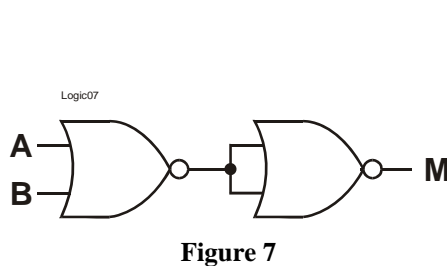| A	B	M(Figure 4)	M(Figure 5)	M(Figure 6)

Figure 7

Figure 8

Table 6

Table of States			
Inputs		Outputs	
A	B	M(Figure 7)	M(Figure 8)

4.   Exclusive-OR Gate and Digital Comparators

Objectives: To investigate the Exclusive-OR function in its gate and comparator forms by observing the tables of states of the 7486 and 7485 devices and relating these to the desired logic operations.

Procedure 3:   The pin out of the 7486 quad, 2-input Exclusive-OR gate is shown in the Appendix (Section 10.3. TTL IC Pin Outs). Determine the table of states (Table 7) for one of the gates. Again, use the Mini-Lab 200 for digital sources and indicators. Record your data as LO and HI (or L and H).
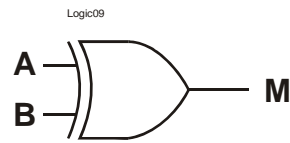
Logic09

Figure 9

Table 7

State Table for Figure 9		
Inputs		Output
A	B	M

Question 7:   Draw an all NAND gate implementation of the Exclusive-OR function.

Question 8:   The equality or coincidence function can be implemented by inverting the output of the Exclusive-OR gate. Implement this with one 7486 gate and one 7404 inverter (see the Appendix for pin outs). Sketch the circuit and fill in the table of states (Table 8 is the prototype).

Table 8

State Table for Equality Gate		
Inputs		Output
A	B	M

Question 9:   Show that the equality condition is indicated at the output of the circuit shown in Figure 10 only when each of the four bits of one of the digital words is equal to the corresponding bit of the second digital word for the combinations in the table.
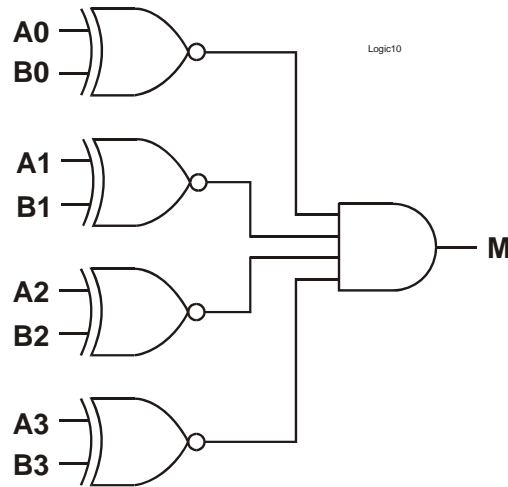
A0
B0

A1
B1

A2
B2

A3
B3

Logic10

M

Figure 10

Table 9

Table of States for Figure 10							
Inputs: Word A				Inputs: Word B			Output
A3	**A2**	**A1**	**A0**	**B3**	**B2**	**B1**	**B0**	**M**
L	H	H	L	L	H	H	L	
L	H	L	L	L	H	H	L	
L	L	H	L	L	H	H	L	

The 7485 magnitude comparator is a medium scale integrated circuit (MSI chip). Its pin out is shown in Appendix. The 7485 performs magnitude comparison of binary and BCD coded digital words.

Procedure 4:   The 7485 comparator is located on the MSI gates job board. Connect the **A** inputs to 4 logic level sources and the **B** inputs to 4 more logic level sources. Connect the **A > B**, **A < B**, and **A = B** outputs to logic sensors. Use several **A** and **B** input combinations and fill in the following table of states.

Table 10

Input Word A				Input Word B				Outputs		
A3	**A2**	**A1**	**A0**	**B3**	**B2**	**B1**	**B0**	**A > B**	**A < B**	**A = B**
L	H	H	L	L	H	H	L			
L	H	L	L	L	H	H	L			
H	H	L	L	L	H	H	L			

Question 10:   Describe the logic in the comparator chip that is needed to obtain the **A = B** output, the **A > B** output and the **A < B** output. Use diagrams and Boolean (i.e. logic) expressions in your description where appropriate.

5.   Adders

Procedure 5:   For this experiment, you will use the basic gates job board. Wire the half-adder shown in Figure 11 using an AND gate and an Exclusive-OR gate on the basic gates job board. Complete the table of states (Table 11). Show that the circuit produces the desired logic function for HI-true signals.
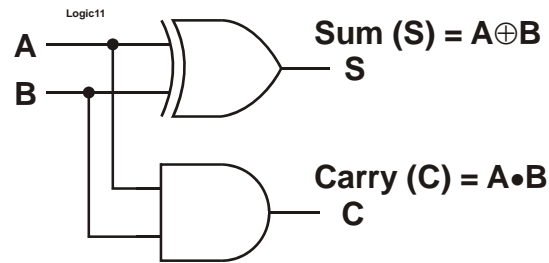
Figure 11

Table 11

Table of States for Figure 11			
Inputs		Outputs	
		Sum	**Carry**
A	**B**	$A \oplus B$	$A \bullet B$

Procedure 6:   Locate the 7483 full adder chip on the MSI gates job board and refer to the pin out in the Appendix. This adder produces a four-bit sum (Σ) and a carry out (**CO**) from 2, four-bit words (**A** and **B**) and a carry in (**CI**).

The table below describes the binary addition of **A** = 10 and **B** = 9 to give a sum=19. In the pin out, the least significant bit (LSB) of a word **A** is designated **A1**, the next most significant bit **A2**, etc.

Table 12

	MSB			LSB	
	4	**3**	**2**	**1**	**CI**
Word A	1	0	1	0	0
Word B	1	0	0	1	0
Sum	0	0	1	1	
Carry out, **CO 1**					

Procedure 7: Use logic level output signals to represent word **A** and word **B**. Wire the signals to the adder inputs according to the pin diagram. Connect the carry in to COMMON to provide **CI** = 0. Connect the sum outputs (1 - 4) and the carry out to logic level sensors. Perform the binary addition of at least five pairs of 4-bit binary numbers and record the results in Table 13. The designated function is performed for HI-true signals only.

Table 13

Word **A**				Word **B**				**Sum**				Carry Out	Decimal Equivalent		
A4	**A3**	**A2**	**A1**	**B4**	**B3**	**B2**	**B1**	**4**	**3**	**2**	**1**	**CO**	Word A	Word B	**SUM**

Procedure 8: Enter another combination of words **A** and **B** in Table 13 and obtain the results for **CI** = 0 (COMMON) and **CI** = 1 (+5V). Enter the results in Table 13.

Question 11: Record your results in your report.

Question 12: Sketch a block diagram of a circuit that uses 7483's to add two 8-bit words.

Question 13:   Two nuclear counters are used, one to count β particles and the other to count γ particles. Parallel digital outputs are available from each counter. A warning signal is desired when the sum of the β and γ particles exceeds a preset binary number. Sketch a block diagram of a circuit to produce the warning signal.

6.   Binary Decoder

Procedure 9:   A binary decoder provides a separate logic level output for all combinations of input logic levels. The binary decoder of Figure 12 decodes the four possible states of the two input signals **E** and **F** into separate output lines **Q**, **R**, **S**, and **T** and is therefore called a 2-line to 4-line binary decoder. Wire the circuit of Figure 12 on the basic gates job board.

Verify the decoder function by filling out the table of states (Table 14).
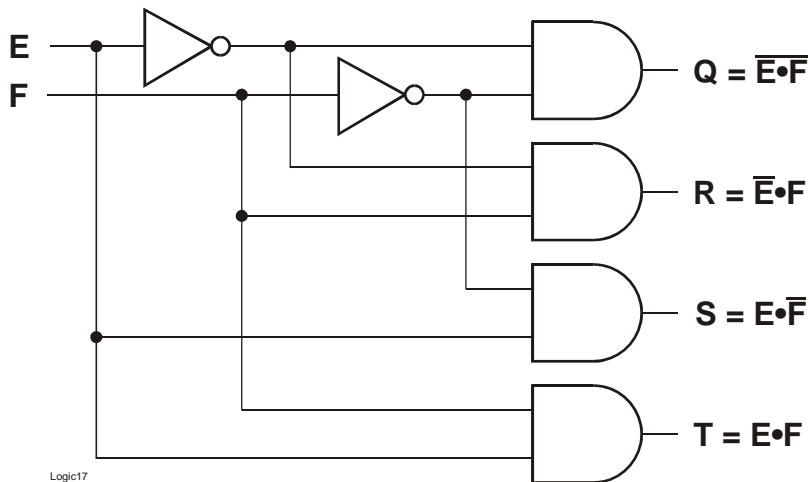
Figure 12

Table 14

Table of States for Figure 12					
Inputs		Outputs			
E	F	Q	R	S	T
L	L				
L	H				
H	L				
H	H				

Question 14:   Transpose the table to your report.

Procedure 10: Locate the 7442 BCD-to-decimal decoder on the MSI gates job board. Refer to the 7442 pin out figure in Appendix and connect four logic sources to the A-D inputs of the chip. Connect each decoder output to a logic level sensor.

Construct a table of states (Table 15) for all input combinations.

Question 15:   What is the significance of the small circle on each output of the pin out?

Question 16:   A digital alarm clock is available with four lines which indicate unit hours in BCD code. If these outputs are connected to the **A-D** inputs of the 7442 decoder and decoder outputs 1 and 5 are connected to the inputs of a NAND gate, predict the hours of the day that the NAND gate output will be HI.

Table 15

Table of States for 7442														
Inputs				Outputs										
D	C	B	A	0	1	2	3	4	5	6	7	8	9

7. Multiplexer

Figure 13 depicts a generic multiplier, a device that allows one of several signals to be selected and forwarded to remaining parts of the circuit. Figure 14 illustrates the implementation of a digital multiplexer with a group of logic gates.

> **Question 17:** Determine the effect of each of the inputs of the multiplexer shown in Figure 13 and Figure 14 upon the output for each of the control settings shown in the table, and record the results. **You need not wire this circuit.**

Figure 13

Table 16

Table of States for Figure 14					
Inputs				Outputs	
a	b	c	d	out	no effect on output
L	L	L	L	L	A,B,C,D
H	L	L	L	A	B,C,D
L	H	L	L		
L	L	H	L		
L	L	L	H		
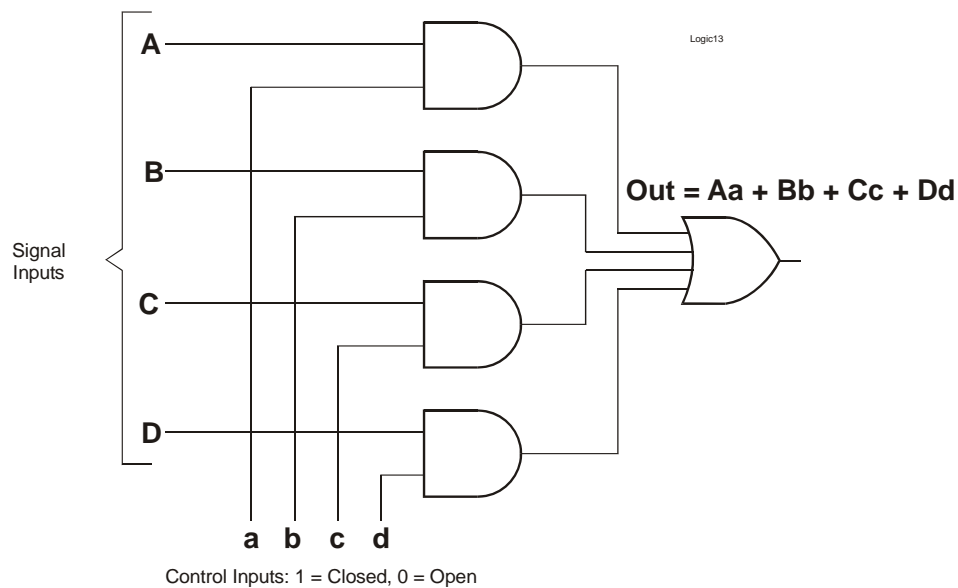
Figure 14

Question 18:   The control inputs of the multiplexer made from basic gates in this manner are cumbersome to use. Describe a circuit that could be added to the simple multiplexer to allow the data channel to be controlled by a two-bit binary number.

Question 19:   A digital time base is composed of a 1.00 MHz crystal oscillator and 3 decade-dividers. Outputs of 1.00 MHz, 100 kHz, 10 kHz, and 1 kHz are available on 4 separate lines. Design a circuit (on paper) to multiplex these outputs and allow switch selection of the frequency. Use basic gates in your design.

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8.   Flip-Flops

Objectives: To investigate the response of flip-flops (FF) to signals at the data, clock, and preset inputs. Also, to appreciate the differences in the responses of representative flip-flop types by observing the behavior of the 7474 edge-triggered D FF, the 7476 level-triggered JK FF.

NOTE: An over scored label such as $\overline{Toggle\ A}$ indicates that the default state for that input is HI and should be set to HI when the circuit is assembled.

NOTE: Signals labeled **_Logic Level i_** will be connected to one of the Digital Outputs of the Mini-Lab 200. Signals labeled **_Logic Sensor i_** will be connected to one of the Digital Indicators of the Mini-Lab 200.

NOTE: Figure 15 shows the Pulser part of the Mini-Lab 200 One Shot section which provides two momentary switches each of which has two sets of output connectors, one labeled **_0_** and one labeled **_1_**. For this unit, **_PulserA₁_** will refer to the **_1_** outputs of the left Pulser, **_PulserB₀_** will refer to the **_0_** outputs of the right Pulser, etc. In this unit, $\overline{Toggle\ A}$ will refer to **_PulserA₁_** , etc.
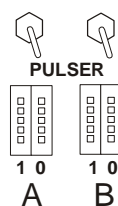
Figure 15 - Mini-Lab 200 Pulser

Procedure 11: Connect the DMM and one of the Mini-Lab 200 Digital Indicators to *PulserA$_1$*. Make the observations indicated in Table 17 and record the data. Repeat with *PulserA$_0$*.

Table 17

	PulserA$_1$		PulserA$_0$	
Table of States				
Switch Position	Voltage	Digital Indicator	Voltage	Digital Indicator
Down (Normal state)				
Up (Hold the switch up while making the observation)				

Procedure 12: Install the Flip-flop Job Board. Locate the 7474 dual D flip-flop. Connect the flip-flop as illustrated in Figure 16 using the pin out diagram in Appendix. Set Logic Level **A** to logic HI and toggle *Toggle A* to clear the flip-flop.
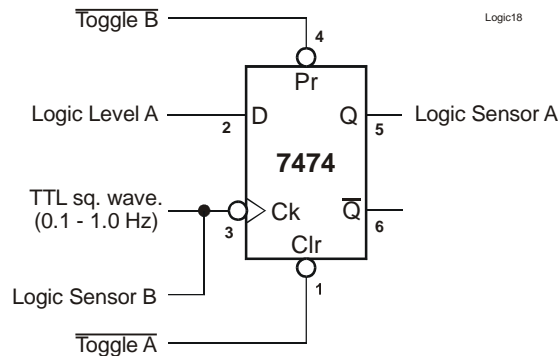
Figure 16

Table 18

FUNCTION TABLE					
INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q$_0$	Q$_0$

Procedure 13: By comparing the time relationships of the **clock (Ck)** (Logic Sensor B) to the **Q** output (Logic Sensor A), note which edge (rising or falling) of the clock causes the information present at the **D** input to be transferred to the **Q** output. Set Logic Level **A** to the LO position and repeat the experiment.

Question 20:   Information at **D** is transferred to **Q** on which edge of the clock?

Which logic level at **Preset** (Pr) causes the Q output level to become set?

Which logic level at **Clear** (Clr) causes the Q output level to become clear?

Are preset and clear dependent on the clock input?

Procedure 14: With a very low frequency clock signal, watch for the **D** input information to be transferred to the **Q** output. Before the next clock transition, change the information at the **D** input to the opposite logic level and note whether the new input information can be transferred before the next appropriate clock edge.

Question 21:   Can the **D** input information be transferred before the clock edge?

Procedure 15: Now the distinction between edge-triggered and level-triggered flip-flops will be drawn by comparing the 7476 JK flip-flop to the 74112 edge-triggered JK flip-flop. Do not use the 74LS76 in this experiment because it is also an edge-triggered flip-flop.

To illustrate this distinction, first wire the 7476 circuit shown in Figure 17. Toggle *Toggle B* to clear the flip-flop. Set the **J** and **K** inputs to LO, and note the effect of toggling **Toggle A**. Set **J** = Hi and **K** = Hi and toggle **Toggle A**.

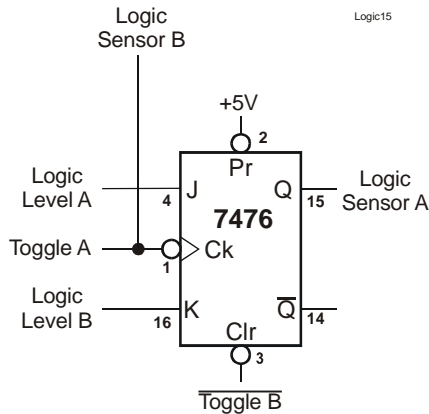**Question 22:**   On which transition of **Ck** does **Q** change states?
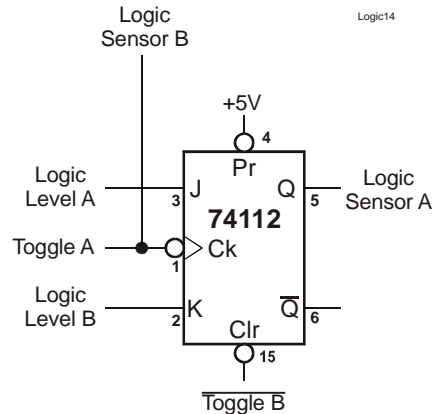

Figure 17

Figure 18

Procedure 16: Clear the flip-flop, and depress and set **Toggle A** to HI. Bring **J** to logic HI and back to logic LO without changing the state of **Toggle A**. Set **Toggle A** to LO and note the effect on **Q**. Note that if **J** is logic HI at <u>any</u> <u>time</u> while the clock is HI, data will be transferred to the output on the falling edge of the clock.

Procedure 17: Disconnect the circuit and wire the 74112 in the same configuration as shown in Figure 18. Repeat the experiment on the loading and transmission of data at the **J** input.

Question 23:   Describe the differences in the behavior of the 7476 and 74112 flip-flops.

9.   Counters
Objectives: To study the counting operation and its implementation with flip-flops and MSI counters by connecting flip-flops into binary up and down counters and by using a 74190 decade counting unit IC as a frequency divider.

Procedure 18: Wire the four-bit binary counter of Figure 19 with the two 7476 dual JK flip-flops on the Flip-Flop Job Board. Use a logic level (**Toggle A**) for the **Count** input, logic level (**Toggle B**) for the **Clear**, and a logic level source for the **Preset** (**Toggle P**). Set **Toggle P** to HI. Clear the register and advance the count. Fill in the count sequence table.
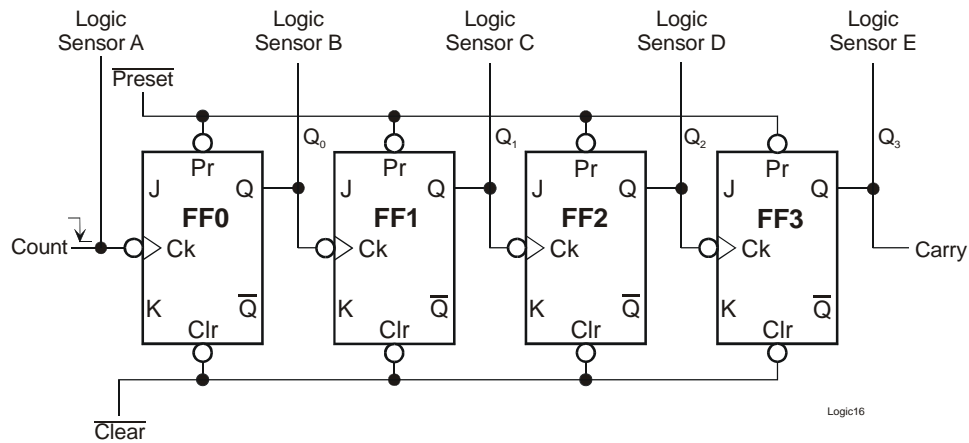

Figure 19

Table 19

Count	Outputs					Count	Outputs			
	Q_3	Q_2	Q_1	Q_0			Q_3	Q_2	Q_1	Q_0
0						8				
1						9				
2						10				
3						11				
4						12				
5						13				
6						14				
7						15				
						16, 0				

Procedure 19: Disconnect **Toggle A** from the **Ck** input of flip-flop 0 and connect in its place a 1 Hz TTL square wave from the Function Generator. Also connect the Function Generator output to a logic level indicator. Momentarily toggle the clear switch (**Toggle B**) and observe the counting through one complete cycle.

Question 24:   On which clock transition does the count advance?

Question 25:   If the change in level at **Q** of each flip-flop occurs 25 ns after the HI->LO transition at T, when does the LO->HI transition occur relative to the trailing edge of the eighth input pulse?

Question 26:   How many binary flip-flops would be required for a counter with a capacity sufficient to count 900 counts?

Procedure 20: Connect Q_3 to the B input of DMM set in frequency mode. Set the Function Generator to 10 kHz and record the frequency ratio f(**Ck**)/f(Q_3). Repeat for Q_2, Q_1, and Q_0.

Table 20

	$f(Ck)$	$f(Q_i)$	$f(Ck)/f(Q_i)$
Q_0			
Q_1			
Q_2			
Q_3			

Question 27:   Record the above table in your report and suggest a practical application for this circuit.

Procedure 21: Disconnect the DMM, but leave the Function Generator, logic level sensors, and logic level inputs connected to the counter.

The next sections will make use of the seven segment LED display on the Counter Job Board. Figure 20 shows details of that display. Such a display provides the display of the decimal digits (0, 1… 8, 9) as shown in Figure 21.
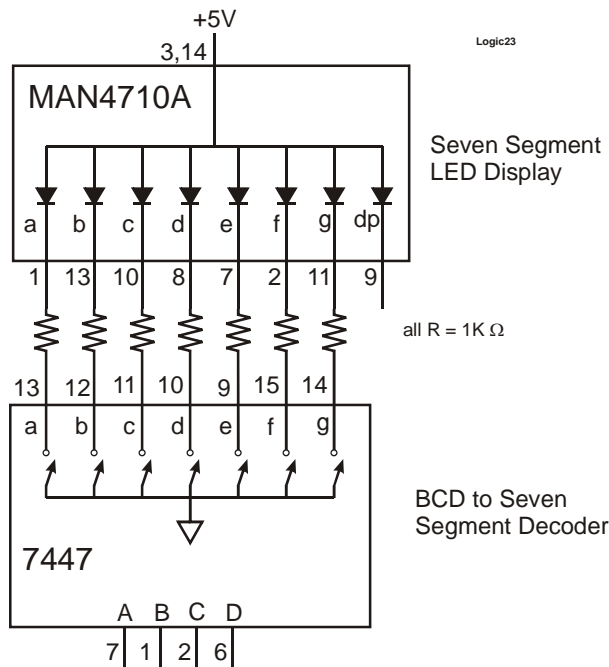
Figure 20

Figure 21

Procedure 22: Next the 74190 decade up/down counter will be studied. Install the Counter Job Board. Wire the decade up/down counter and display circuit shown in Figure 22.
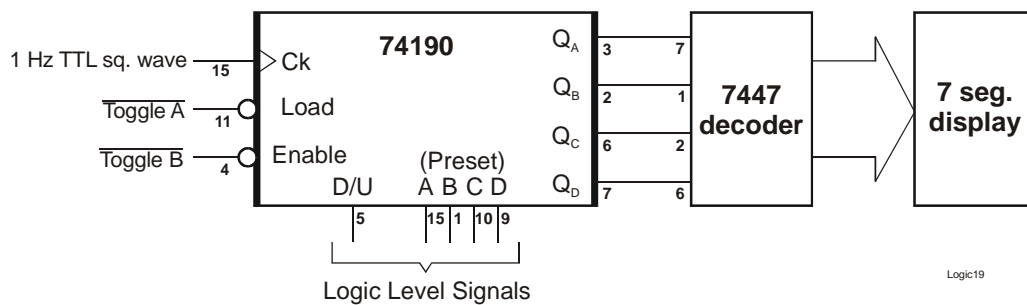
Figure 22

Procedure 23: Set the preset switches to HLLH and load the data. Observe the count and demonstrate that the data can be loaded at any point during the count sequence. Note the effect of the down/up (**D/U**) control. Load several numbers into the counter and observe the results.

Question 28: Note that the 74190 has no external clear input. Suggest a method to clear the counter.

Does the loading occur synchronously with the clock?

Determine the frequency in Hz of each of the counter outputs relative to the clock input for several clock frequencies between 1 kHz and 100 kHz.

Table 21

Clock	Q_A	Q_B	Q_C	Q_D

Procedure 24: Leave the decoder and seven segment display connected to the 74190 for the following experiment.

Procedure 25: Next the 74190 will be reconnected to form a variable modulus counter. As shown in Figure 23, the IC counter is wired as a down counter with a gate at the output to detect a zero count and preset the counter to a desired modulus. The gate at the output of the counter can be constructed from equivalent gates on the Basic Gates Job Board.
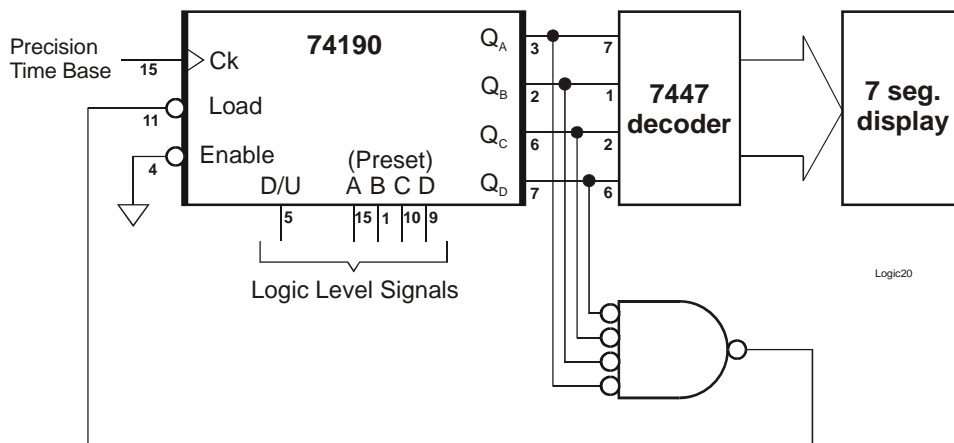
Figure 23

Question 29: List the IC gates that you plan to use to implement the OR function.

Procedure 26: Set the time base to 1 Hz, set the **U/D** control for down counting, and set the preset levels to LHLH. Observe and describe the behavior of the counter for this preset value and several others.

Question 30: Why is this circuit called a variable modulus counter?

Procedure 27: Now use the 100 kHz output of the time base as the **Ck** input to the counter, and measure the frequency of the load pulses as a function of the magnitude of the number at the preset input. Complete the table for several preset values.

Table 22

Preset Data				f(load)
L	L	L	L	
H	H	H	H	

Question 31: Determine what happens if numbers outside the range 0-9 are applied to the preset input. Explain.

Question 32: It is desired to produce a clock with selectable periods of 100 ms, 200 ms, 300 ms, 400 ms, and 500 ms. Design in block diagram form a circuit made from two 74190's that provides these periods. The preset control should read directly in hundreds of milliseconds. Do the periods have 50% duty cycles?

10.   Appendix

10.1.   Boolean Algebra (An Introduction)

Operators		
AND	$A \bullet B$	
OR	$A + B$	
NOT	$\overline{A}$	
AND Theorems	$0 \bullet 0 = 0$	$A \bullet 0 = 0$
	$1 \bullet 1 = 1$	$A \bullet A = A$
	$1 \bullet 0 = 0$	$A \bullet \overline{A} = 0$
	$A \bullet 0 = 0$	
OR Theorems	$1 + 1 = 1$	$A + 0 = A$
	$0 + 0 = 0$	$A + A = A$
	$0 + 1 = 1$	$A + \overline{A} = 1$
	$A + 1 = 1$	
NOT	$\overline{\overline{A}} = A$	
Commutation	$A + B = B + A$	$A \bullet B = B \bullet A$
Absorption	$A + A \bullet B = A$	$A \bullet (A + B) = A$
Association	$A + (B + C) = (A + B) + C$	$A \bullet (B \bullet C) = (A \bullet B) \bullet C$
Distribution	$A + B \bullet C = (A + B) \bullet (A + C)$	$A \bullet (B + C) = A \bullet B + A \bullet C$
DeMorgan's Theorem	$\overline{A + B} = \overline{A} \bullet \overline{B}$	$\overline{A \bullet B} = \overline{A} + \overline{B}$

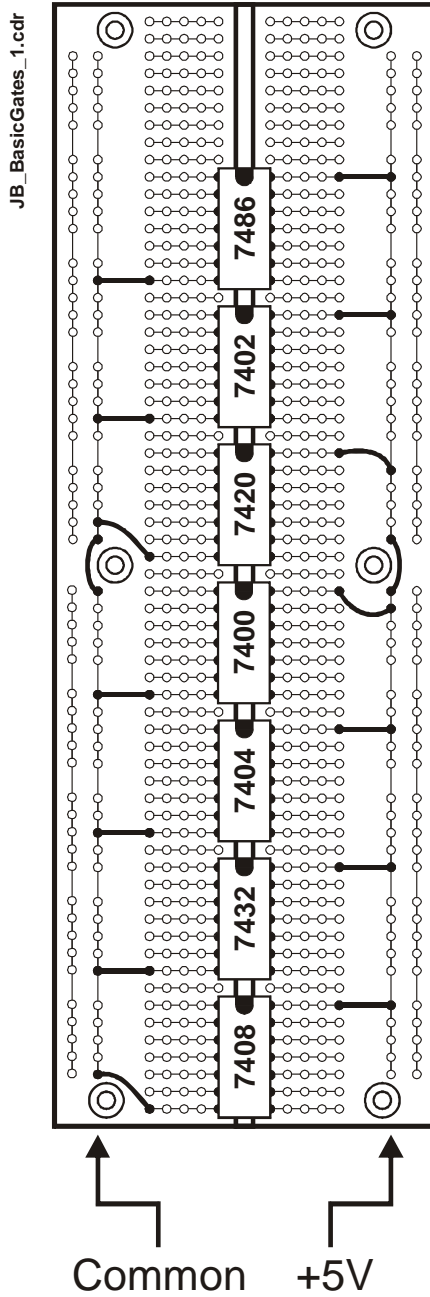## 10.2. Logic Job Boards

Basic Gates Job Board

Figure 24 - Basic Gates Job Board

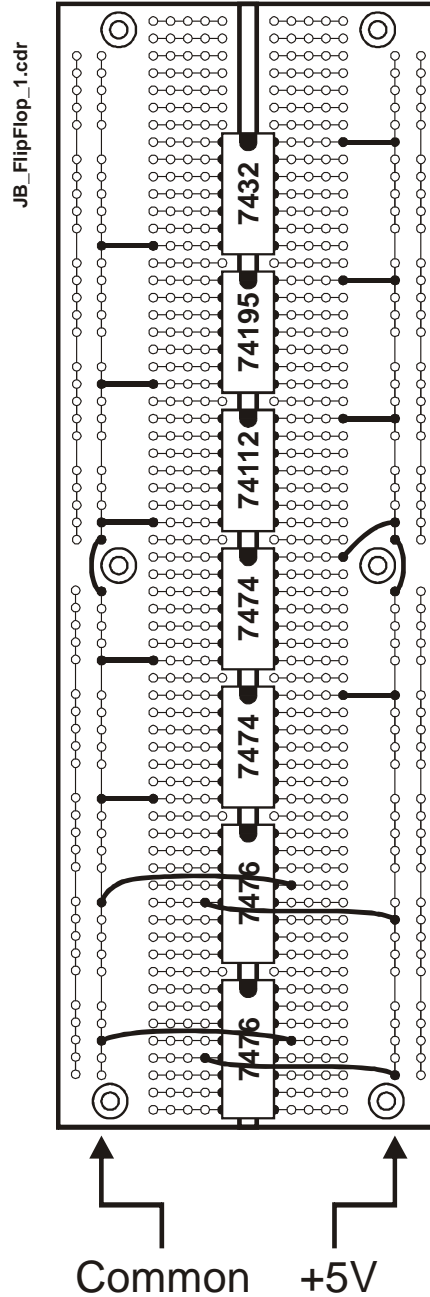**Flip-Flop Job Board**

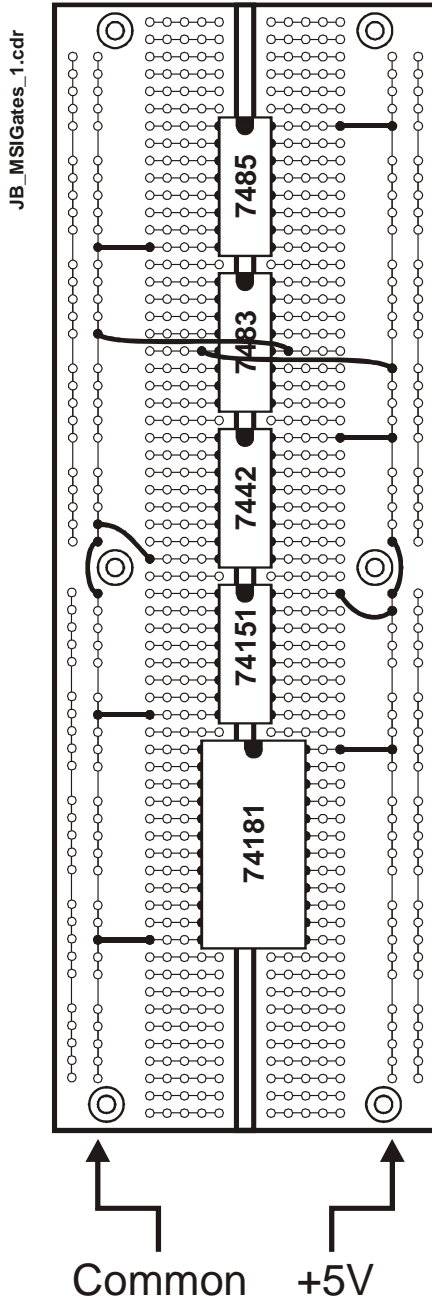**Figure 25 - Flip-Flop Job Board**

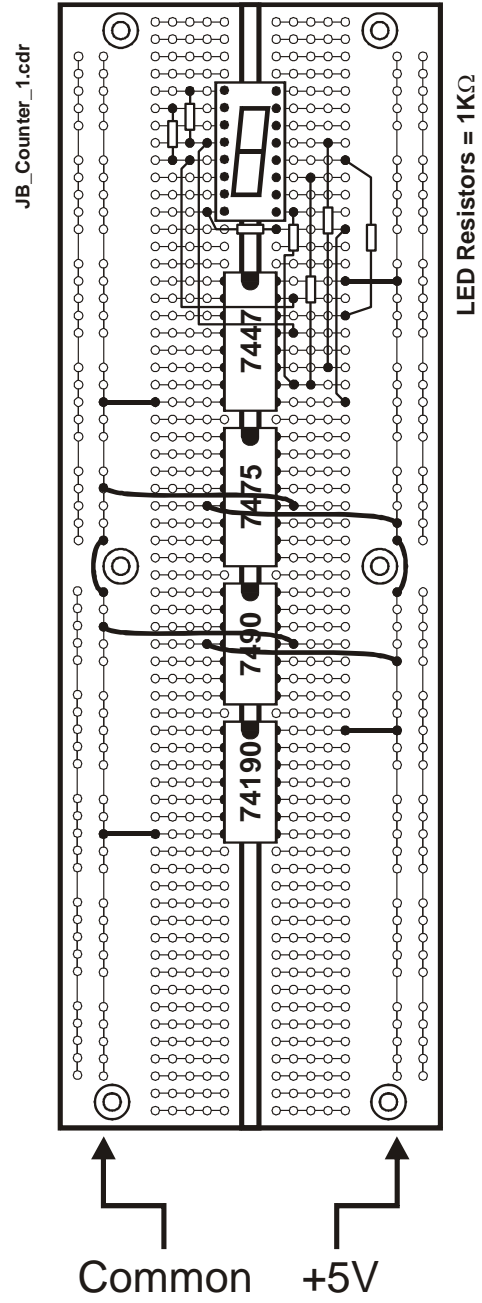## MSI Gates Job Board

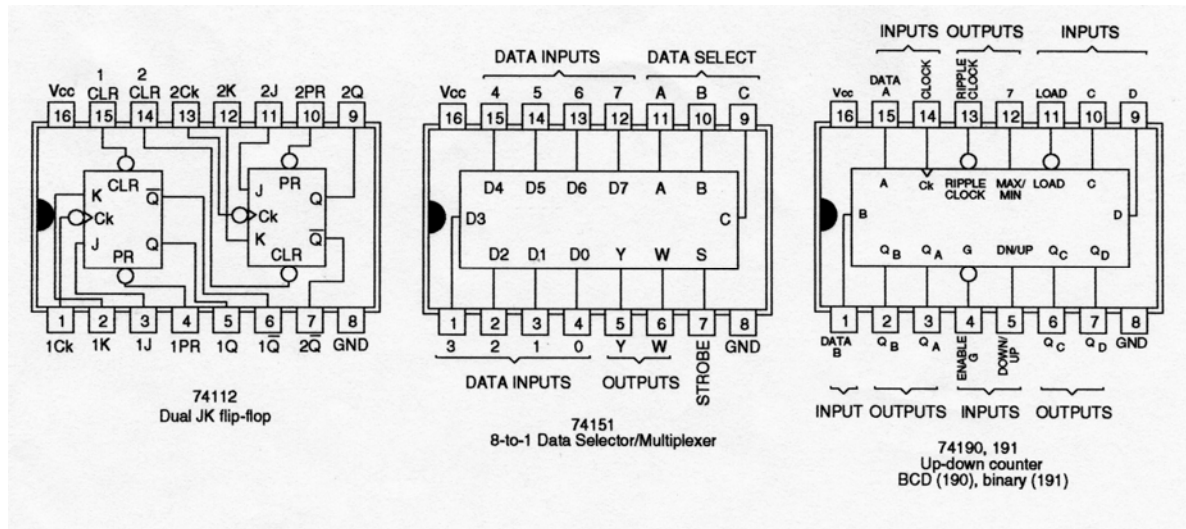**Figure 26 - MSI Gates Job Board**

Counter Job Board

Figure 27 – Counter Job Board

10.3. TTL IC Pin Outs

7400, 03, 26, 37, 38
Quad NAND

7402, 28, 33
Quad NOR

7404, 05, 06, 16
Hex INVERT

7408, 09
Quad AND

7420, 22, 40
Four-input NAND

7432
Quad OR

7442
BCD Decoder

7474
Dual D flip-flop

7476
Dual JK flip-flop

7483
4-Bit Full Adder

7485
4-bit Comparator
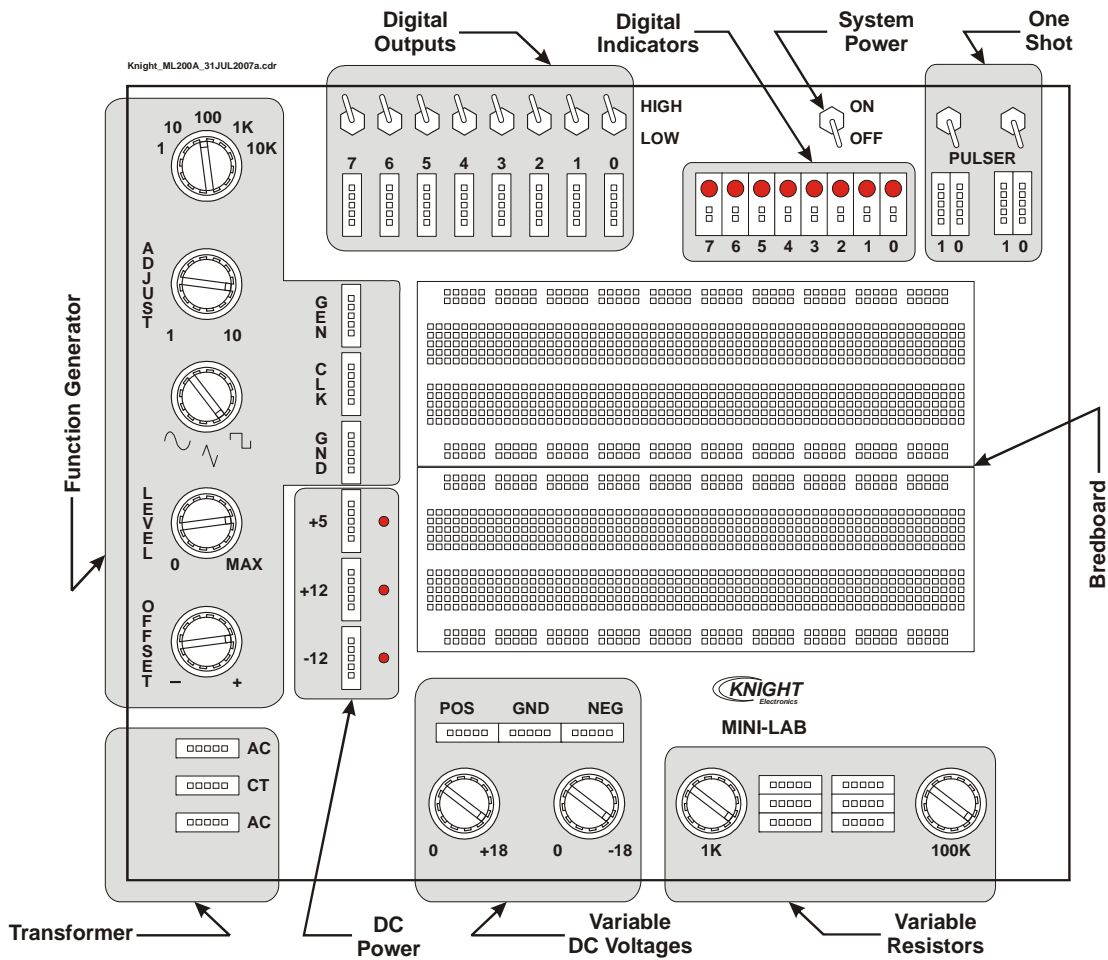
7486
Exclusive-OR
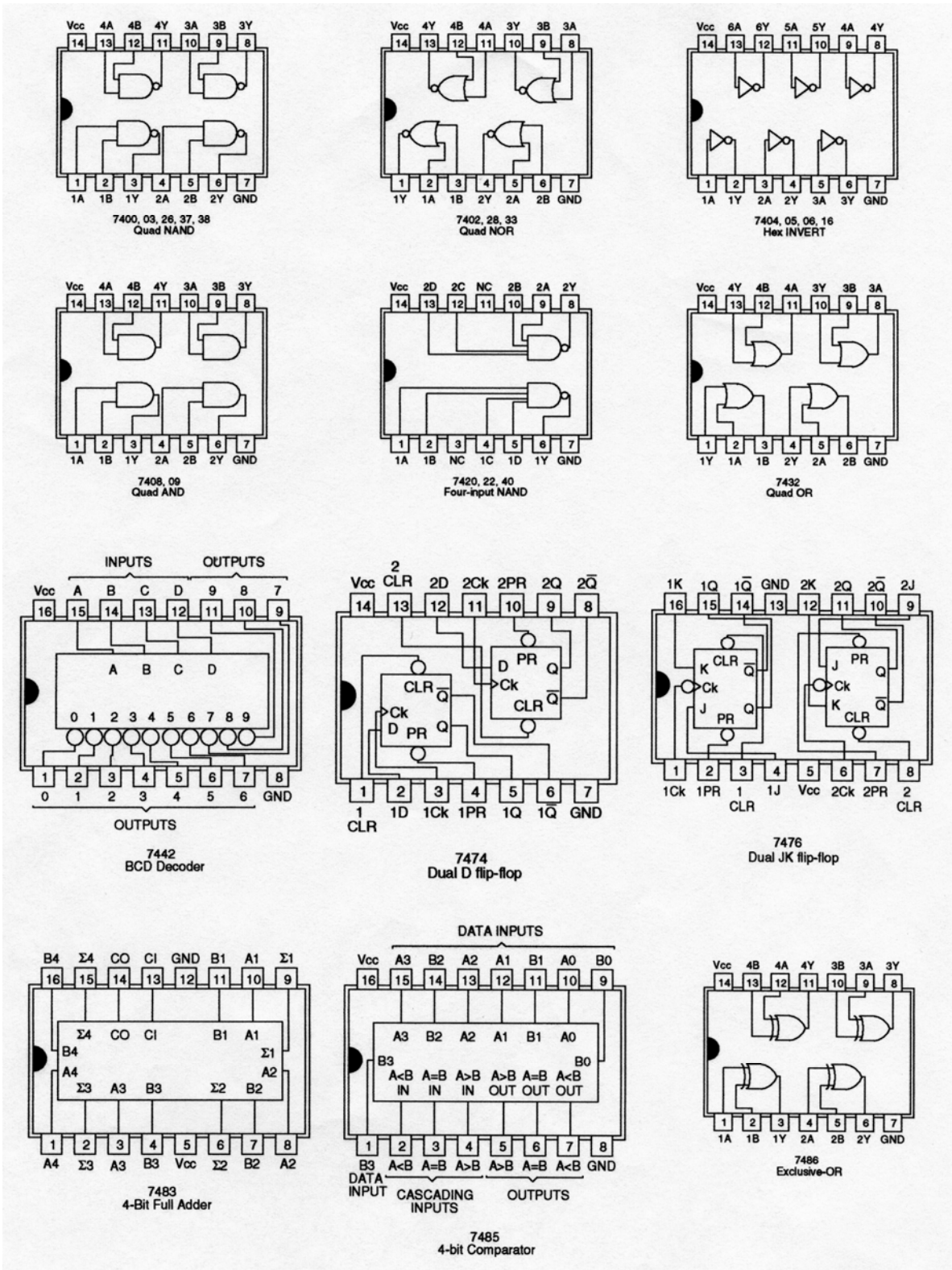
10.4. Knight Mini-Lab 200

Figure 28 - Mini-Lab Work Station

10.5. Material Required For This Unit

Quantity	Value	Description
1	47 Ω	Resistors
1	10 Ω	Resistors
1	470 Ω	Resistors
1		Counter Job Board
1		Basic Gates Job Board
1		MSI Gates Source
1		Flip-flop Job Board
1		Mini-Lab 200
1		DMM
1		Oscilloscope
1	7400	7400
1	7420	7420
1	7402 quad	7402 quad
1	7486 quad	7486 quad
1	7485	7485
1	7404 inverter	7404 inverter
1	7483 full adder chip	7483 full adder chip
1	7442 BCD-to decimal	7442 BCD-to decimal
1	7474 edge-triggered D FF	7474 edge-triggered D FF
2	7476 JK flip-flop	7476 JK flip-flop
1	74112 edge triggered JK flip-flop	74112 edge triggered JK flip-flop
1	74190	decade counting unit IC
1	7447 decoder	decoder
1	7 seg display	7 seg display

11.   Revision History

Revision History for Digital Logic Unit

Revision	Date	Authors	Description
1.0	Fall 1992	E. C. Hemenway	First edition. Used Fall 92.
2.0	14-Nov-1993	E. C. Hemenway, T V Atkinson	Changes from first time the course was offered. Used Fall 93.
2.1	13-OCT-1994	T V Atkinson	Now Unit 8. Old Unit 7. Renumbered due to splitting old Unit 4 into two units.
2.2	11-Nov-1996	J. Allison, S. Crouch	Grammatical changes, renumbering figures
3.0	11/23/98	T. Cullen	Conversion to LabWindows/CVI. Reformatting.
4.0	12/8/98	S.R. Crouch T. F. Cullen	Streamlined unit. Deleted repetitive and redundant experiments.
5.0	Sep-2000	T V Atkinson	Renamed to be Unit 6
5.1	Oct 2001	T V Atkinson, Jose-Luis Gallegos-Perez	Added details of the seven segment LED display, list of materials.
5.2	Oct 12, 2005	T V Atkinson	Corrected Figure 6-9, the Exclusive Or gate.
5.3	29-Oct-2007	T V Atkinson	Changed to the Mini-Lab 200.
5.3e	29-Oct-2007	T V Atkinson	Corrected the power and ground connections on the Flip-Flop Job Board.